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Electrical Properties of p-Type $GaInP_2$

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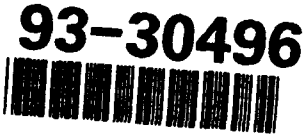

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Electrical Properties of p—type $GaInP_2$

THESIS

Presented to the Faculty of the Graduate School of Engineering

of the Air Force Institute of Technology

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Master of Science in Applied Physics

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Captain, USAF

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Preface

The purpose of this study was to determine some of the basic properties of p—type $GaInP_2$ that had not been examined up until now. The current need for this information is to determine the suitability of $GaInP_2$ for use as a high-efficiency solar cell material for satellites and terrestrial use.

Extensive deep level transient spectroscopy (DLTS) studies of n^+—p $GaInP_2$ diodes were performed with a variety of parameters. The two most important parameters were the doping concentration of the p-side of the diode, and the fluence of 1 MeV electron irradiation the diode received. 1MeV electron irradiation was chosen in order to study the effect of long term exposure to the space environment.

This study is not the work of just myself. I am deeply indebted to my advisor, Dr. Y. K. Yeo, for his continual support and encouragement. I wish to thank Mrs. Bonnie Riehl for her outstanding dedication and for her assistance in learning to use the equipment. I also owe a debt of thanks to Mr. Kitt Reinhardt for his knowledge and supply of the diodes and his invaluable assistance. Additionally, my thanks to Captain Dan Johnstone for his help in learning to use the DLTS equipment and writing the controlling DLTS and CV programs. I would also like to thank my classmates and their spouses for all the fun, adventure and learning. Finally, I wish to thank my family, Robert and Q, for keeping me in touch with reality.

Roy S. Calfas

Abstract

The $GaInP_2$ n^+—p junction diode has recently become important to the development of high efficiency $GaInP_2$ /GaAs dual junction solar cells, which have a demonstrated air mass 1.5 conversion efficiencies in excess of 27%. In order to study the effects of long term exposure to the space environment, the $GaInP_2$ n^+—p junction diodes were irradiated with a 1 MeV electron beam with a fluence of 10^{16} electrons/cm^2. Since little is known about deep level defects (traps) in $GaInP_2$, a deep level transient spectroscopy (DLTS) study was made to characterize the traps that are thought to dominate the dark current in $GaInP_2$ solar cells. The measurements indicated that there are a number of majority carrier traps in the p-type base of the $GaInP_2$ n^+—p junction diode. Traps that are identified are located 0.12 to 0.55 eV above the valence band and are attributed to phosphorous vacancies in the lattice.

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1. Introduction

Current satellite launch technology is fundamentally limited by its payload-to-orbit rating. The higher the orbit, the lower the payload mass. A significant contribution to satellite mass is the solar cell array needed to power the equipment throughout its anticipated lifetime. A highly efficient solar cell which is also highly resistant to radiation induced defects can be much smaller for a given power than current silicon cells. A smaller solar cell array leads directly to a smaller payload percentage devoted to power generation. Solar cells using alloys of GaAs and InP are known to have high efficiencies and high radiation resistance compared to Si solar cells.(Reinhardt:1992) This then allows for either a higher orbit from a given launch vehicle or a greater proportion of satellite mass devoted to instruments or other productive elements. $GaInP_2$ has been proposed as a high-efficiency, long lifetime material for solar cells.(Cavicchi:1991) However, very little is known about the electrical properties of $GaInP_2$ and especially the electron irradiated $GaInP_2$. Specifically, the deep level defects which are thought to dominate the dark currents in $GaInP_2$ n^+-p solar cells are not well characterized.

1.1 Problem Statement

While $GaInP_2$ has been suggested for the role of a efficient, lightweight solar cell, very little is known about its electrical properties in general or in the space environment where electron irradiation is significant. Some work has been done on the bulk electrical properties of $GaInP_2$ at high temperatures (Zhu:1990). Some of the work performed here on $GaInP_2$

has been done previously (Zhu:1990), and for InP (Messenger:1992). Despite the previous work, nothing is known about the dark currents in $GaInP_2$ solar cells. It is these dark currents that limit the performance of a solar cell. Previous work at the Air Force Institute of Technology (Reinhardt:1992) has shown that dark currents in $GaInP_2$ n^+-p diodes is dominated by recombination of electron hole pairs (carrier recombination). Carrier recombination is assisted by deep level defects. It is the characterization of these defects in p—type $GaInP_2$ that is the subject of this thesis

1.2 Sequence of Presentation

Before proceeding with the discussion of the electrical properties of $GaInP_2$, it is essential to be aquatinted with relevant semiconductor basics and the effect of impurities and defects in the band gap. Thus, Chapter 2, **Electron States in Semiconductors**, a general overview of electron states in the band gap, and transitions between them and the bands, will be presented. In Chapter 3, **Deep Level Transient Spectroscopy (DLTS)**, the method used to determine the electrical properties will be discussed. Metal Organic Chemical Vapor Deposition (MOCVD), the method used to grow $GaInP_2$ is the purview of Chapter 4, **Sample Growth and Preparation**. The results of the characterization techniques is given in Chapter 5, **Results and Discussion**. Chapter 6, **Summary**, summarizes the work accomplished for this thesis study and gives recommendations for further study.

2. Electron Levels in Semiconductors

The periodic arrangement of atoms in a crystal gives rise to a discrete energy band structure. Between these energy bands are forbidden regions where no electron states exist. In a conductor, the highest energy band that contains electrons is only partially filled. It is the availability of empty states in the same band that gives rise to a conductor's electrical properties. In an insulator, all energy bands that contain electrons are completely filled. Since there are no available states for electrons to move into, there is no electrical current and the next available band is too high in energy to be accessible. At absolute zero, a semiconductor's electrons are distributed similar to the insulator at room temperature and there are no available empty electron states in the highest energy band that contains electrons. However, the forbidden band in a semiconductor is narrow enough such that thermal excitation can move electrons into the formerly empty upper *conduction* band. This gives rise to conduction from two sources: the electron in the conduction band and the empty state ***hole*** in the lower *valence* band.

The conduction properties of semiconductors can be altered by the introduction of impurities into the crystalline structure. Section 2.1 discusses these acceptors and donors. The occupancy of electron states is the subject of Section 2.2.

2.1 Acceptor and Donor States

The introduction of impurity atoms into the nearly perfect crystalline structure of semiconductors may provide a bound state that lies within the

band gap. The determination of the label, acceptor or donor, is dependent upon the atom's behavior. If the atom has one or more fewer valence electrons than silicon, it acts as an acceptor since it will *accept* and bind one or more electrons from the valence band, thereby producing a conducting hole in the valence band. Conversely, an atom that has more valence electrons than silicon is a donor since it *donates* electrons to the conduction band. As a rough rule, atoms that create electron states in the lower half of the band gap will be acceptors and atoms that create electron states in the upper half of the band gap will be donors. For example, the acceptor in p—type $GaInP_2$ used in this study is zinc. Figure 2.1 illustrates these concepts.

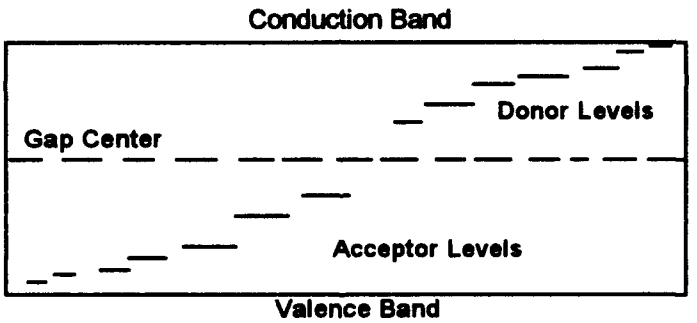

Figure 2.1. Acceptor and Donor States in Semiconductors.

The label "deep level" is somewhat nebulous. A deep level is one that is "far" above the valence band edge or "far" below the conduction band edge. The closer a deep level is to the band gap center, the more efficient it is at assisting carrier recombination. This is the effect that is thought to dominate the dark current in $GaInP_2$ diodes.(Reinhardt:1992)

2.2 *Occupancy of Electron States*

David Look has developed a concise presentation of electron state occupancy for semiconductors. He begins with the occupancy, n_{ijk}, of the k^{th} excited level of the j^{th} charge state of the i^{th} center. The occupancy n_{ijk} is given by

$$n_{ijk} = \frac{N_i}{1 + \sum'_{j',k' \neq j,k} \frac{g_{ij'k'}}{g_{ijk}} \exp\left\{\frac{E_{ij'k'} - E_{ijk} - (j-j')E_F}{kT}\right\}}, \tag{2.1}$$

where the prime indicates the summation, N_i is the total number of the i type centers, E_F is the Fermi energy, g_{ijk} is the degeneracy of the state ijk and E_{ijk} is its energy. Both energies E_F and E_{ijk} are measured from the valence band edge (maximum or upper edge), E_v.

The Fermi energy can not be immediately calculated from Equation 2.1. It is through the requirement of charge neutrality that E_F can be calculated. First, the hole and electron (p and n) carrier concentrations are approximated using Boltzmann distributions. These approximations are

$$p = \frac{2\left(2\pi m_h^* kT\right)^{\frac{3}{2}}}{h^3} \exp\left\{\frac{E_v - E_F}{kT}\right\} = N_v \exp\left\{\frac{E_v - E_F}{kT}\right\} \tag{2.2}$$

and

$$n = \frac{2\left(2\pi m_e^* kT\right)^{\frac{3}{2}}}{h^3} \exp\left\{\frac{E_F - E_C}{kT}\right\} = N_c \exp\left\{\frac{E_F - E_C}{kT}\right\}, \tag{2.3}$$

where m_h^* and m_e^* are the effective hole and electron masses. The total charge, positive and negative is given by

$$Q_p = p + \sum_{i,j=0,k}^{j=j_{Di}} \left(j_{Di} - j\right) n_{ijk} \tag{2.4}$$

and

$$Q_n = n + \sum_{i,j=j_{Di},k}^{j=j_{Di}+j_{Ai}} \left(j - j_{Di}\right) n_{ijk}, \tag{2.5}$$

where Q represents the total charge of holes (p) and electrons (n), and the i, j and k are as in equation 2.1. By requiring charge neutrality, $Q_T = 0$, an equality between n and p can be made

$$n = p + \sum_{i,j=0,k}^{j=j_{Di}+j_{Ai}} \left(j_{Di} - j\right) n_{ijk}. \tag{2.6}$$

For a given temperature, the Fermi energy is the energy at which Equation 2.6 holds true.

Again, Look has considered what happens when one center dominates the behavior of the semiconductor, which is generally the case. In this case, the Fermi energy is determined, at all temperatures, by the one dominant center. With the Fermi energy near the one center, any centers below E_F by more than a few kT are nearly always occupied and those more than a few kT above the Fermi Level are nearly always empty. When this is true, Equation 2.6 reduces to Equation 2.7

$$n + N_A^{net} = \frac{N_D}{1 + \frac{n}{\Phi_D}}, \tag{2.7}$$

where Φ_D is given by

$$\Phi_D = \frac{g_{D0}}{g_D} N_C \exp\left\{\frac{-E_D}{kT}\right\} \tag{2.8}$$

$$= \frac{g_{D0}}{g_D} N_c' \exp\left\{\frac{-\alpha_D}{k}\right\} T^{\frac{3}{2}} \exp\left\{\frac{-E_{D0}}{kT}\right\}, \tag{2.9}$$

where $N_C' = 2(2\pi m_e^* k)^{3/2}/h^3$, the g 's are the degeneracies of the donor energy levels E_D and E_{D0} and α_D is part of the linear dependence of the donor activation energy. The linear dependence of the donor activation energy, $E_D = E_{D0} - \alpha_D T$, is allowed. Unlike previous energies, E_D is measured down from the bottom of the conduction band, E_C. The term N_A^{net} represents the total temperature dependent charge due to other

levels, donor or acceptor, either above or below the Fermi energy. N_A^{net} is given by

$$N_A^{net} = \sum_{i,E_{Ai}<E_F} N_{Ai} - \sum_{i,E_{Di}>E_F} N_{Di}, \tag{2.10}$$

where $N_{A\,i}$ and $N_{D\,i}$ represent the total charge in the i^{th} acceptor and donor levels and $E_{A\,i}$ and $E_{D\,i}$ are the energies of the i^{th} acceptor and donor levels.

For the p—type $GaInP_2$ in this study, the similar equation derived from Equation 2.6 is

$$p + N_D^{net} = \frac{N_A}{1 + \frac{p}{\Phi_A}}, \tag{2.11}$$

where

$$\Phi_A = \frac{g_{A1}}{g_{A0}} N_V' \exp\left\{\frac{-\alpha_A}{k}\right\} T^{\frac{3}{2}} \exp\left\{\frac{-E_{A0}}{kT}\right\}, \tag{2.12}$$

where $N_V' = 2(2\pi m_h^* k)^{3/2}/h^3$, the g's are the degeneracies of the acceptor energy levels E_A and E_{A0} and α_A is part of the linear dependence of the acceptor activation energy. The linear dependence of the acceptor activation energy, $E_A = E_{A0} - \alpha_A T$, is allowed. The term N_A^{net} represents the total temperature dependent charge due to other levels, donor or acceptor,

either above or below the Fermi energy as defined in Equation 2.10. The main differences between Equation 2.12 and 2.9 is the appropriate conduction (N_C') and valence (N_V') effective density of states equations are used and the degeneracy ratios are inverted since the temperature dependent acceptor activation energy E_A generally lies above the temperature independent acceptor activation energy E_{A0} which is the inverse of the donor case. With an understanding of the occupancy of states, a discussion of the characterization techniques can begin in Chapter 3.

3. Deep Level Transient Spectroscopy (DLTS)

Measurements of the small-signal capacitance of a reverse-biased semiconductor p—n junction and of its steady-state and transient change with applied bias and temperature allow considerable quantitative information to be obtained on the doping concentration and its variation with spatial distance, and on the existence, energy levels and concentrations of deep level electron and hole traps in the semiconductor.

3.1. Energy-Band Bending and Depletion Regions

The capacitance characterization technique relies on the properties of semiconductor to semiconductor rectifying junctions like the p—n junction. McKelvey, Sze, Lang, Johnson, Hanak and Miller all provide superb developments which are reviewed here in a condensed form. Figure 3.1a shows the electron energies of the valence and conduction band of a semiconductor for separated p—type and n^+—type samples. In Figure 3.1b, the same is shown after contact and formation of an n^+—p junction. The major effect of interest here is that for the n^+—p junction, diffusion of holes from the p region into the n^+ region and of electrons in the opposite direction has resulted in the setting up of an equilibrium "built-in" potential, V_{bi}, across the junction with the n^+ region positive with respect to the p region. Also, a new region has been formed around the junction which is characterized by the depletion of carriers in both the $n^+$and p regions. At equilibrium, the Fermi Energy level is a constant energy level across the junction, and it is this condition that determines the

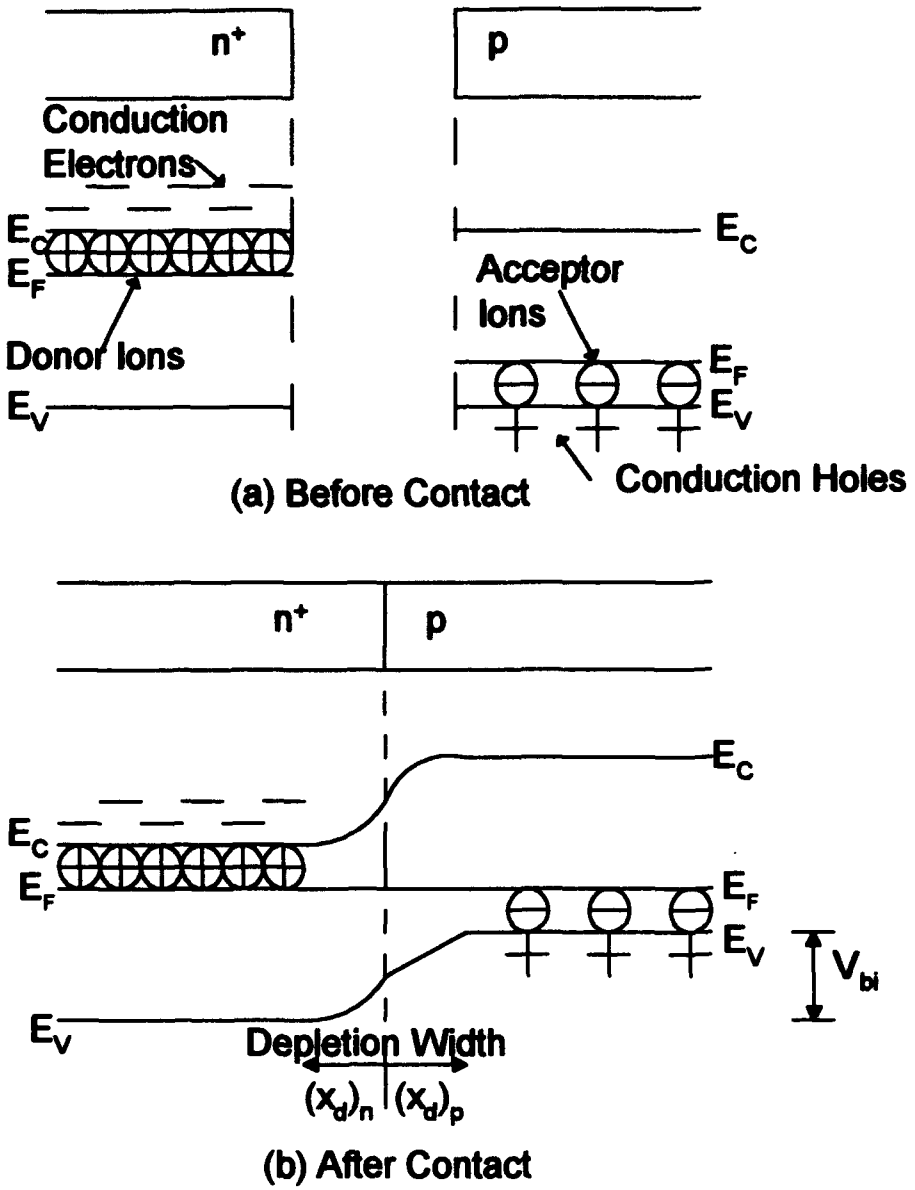

Figure 3.1. Electron energies as a function of distance in an n^+—p junction.

value of V_{bi}. The potential, V_{bi}, is the sum of the component potentials $(V_{bi})_n$ and $(V_{bi})_p$ across the depletion region formed in the n-type and p-type regions contains a space charge due to the individual, immobile doping ions which in turn gives rise to an electric field. Through Poisson's Equation and assuming an abrupt junction, the expressions for $(x_d)_n$ and $(x_d)_p$ can be shown to be of the form

$$\left(x_d\right)_n = \sqrt{\frac{2\kappa\varepsilon_0\left(V_{bi}\right)_p}{eN_A}} \tag{3.1}$$

and

$$\left(x_d\right)_p = \sqrt{\frac{2\kappa\varepsilon_0\left(V_{bi}\right)_n}{eN_D}}, \tag{3.2}$$

where κ is the relative dielectric constant for the material, ε_0 is the permittivity of free space and N_A and N_D are the acceptor and donor impurities for the p—type and n—type regions, respectively. Clearly, if one region is more heavily doped than the other, the depletion region can become very one-sided. In the case of the n^+—p junctions used in this study, almost all of the depletion width and total built-in potential occur in the p—side. For such a one-sided junction, the relationship between the total built-in depletion width $(x_d)_{bi}$ and the total built-in potential V_{bi} is given by

$$\left(x_d\right)_{bi} = \sqrt{\frac{2\kappa\varepsilon_0 V_{bi}}{eN_A}}. \tag{3.3}$$

The charge Q that can be stored in the depletion region under a reverse bias (V_a) condition, provided that N_A is uniform throughout the p—type region, is very simply $N_A x_d A$ where A is the area of the junction. Using Equation 3.3 and realizing that the potential is no longer just V_{bi} but (V_{bi}+V_a), Q is then given by

$$Q = N_A x_d A = A\sqrt{2\kappa\varepsilon_0 eN_A\left(V_{bi} + V_a\right)} \tag{3.4}$$

and the resulting capacitance is

$$C = \frac{dQ}{dV_a} = \kappa\varepsilon_0 \frac{A}{x_d} \tag{3.5}$$

which is exactly the formula for a parallel plate capacitor of inner-plate separation x_d.

Because the data obtained in capacitance based techniques is heavily dependent upon the linear depth of the depletion region, the use of a one-sided junction is of great benefit experimentally since it will be clear on which side of the junction the semiconductor is being tested.

3.2 *Theory of Deep Level Transient Spectroscopy (DLTS)*

DLTS depends on the principle that thermally exciting electron or holes out from traps in a semiconductor junction held in reverse bias leads to movement of those released charges into the external circuit. The number of electrons or holes released from the traps per second depends on temperature, and decays exponentially with time as the traps become progressively empty. Measuring the decay time as a function of temperature allows the transition energy, $E_{tr}-E_v$ in the case of a hole trap (Figure 3.2) or E_c-E_{tr} in the case of an electron trap, to be determined. The release of the trapped charges can be observed experimentally as a transient change in the junction capacitance. The crucial feature of the DLTS technique is that the filling and emptying of the traps is arranged to be repetitive and this permits very sensitive experimental measurement of the capacitance transients by a capacitance bridge.

The temperature of the device is assumed to be high enough that the time for the release of holes from the traps is fairly short, on the order of 10 ms. Figure 3.2 shows a very simple schematic of the origin of the capacitance transient. In Figure 3.2a, a reverse bias, V_{r1}, is being applied across the junction and the depletion width, x_{d1}, is almost entirely in the p—side. During equilibrium, the traps at $x > x_{d1}$ are filled because of the high density of holes in that neutral region. However, those within the depletion region ($x < x_{d1}$) are empty and the capacitance, C_1, is given by Equation 3.5. At time $t = 0$, the applied reverse bias is increased to V_{r2}

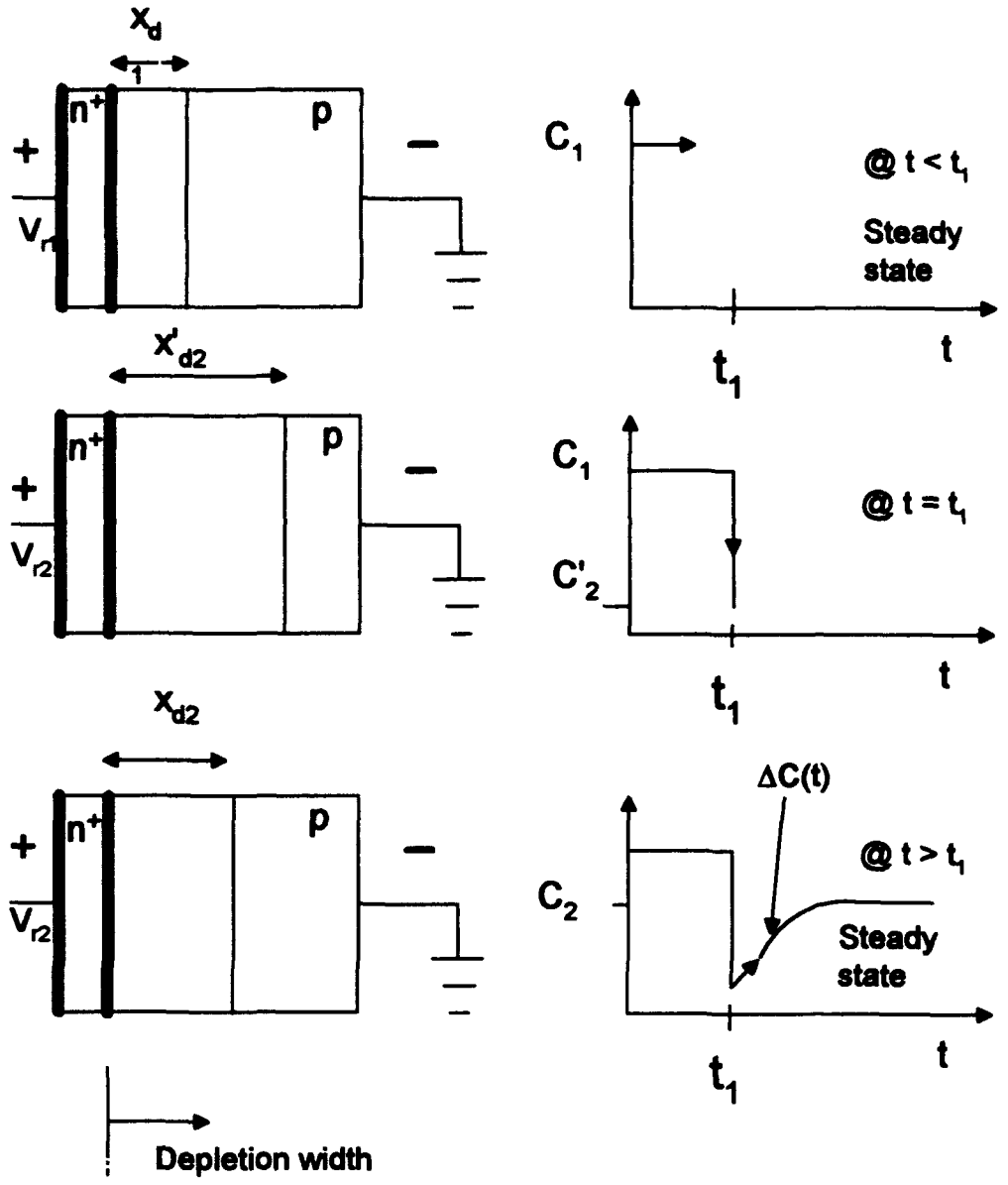

Figure 3.2. Variation with time of the capacitance of a one-sided n^+-p junction following the increase in the applied reverse bias voltage from V_{r1} to V_{r2}.

with the effect that the depletion width increases to x_{d2} and a resulting decrease in capacitance, C_2, as shown in Figure 3.2b. Now, the holes in the region between x_{d1} and x_{d2} are no longer in equilibrium and thermally induced emission of holes into the valence band begins. In turn, this leads the space charge in the new part of the depletion region to increase and the capacitance progresses towards C_2, the equilibrium capacitance for the applied reverse bias V_{r2}. The overall effect being that a capacitance transient, $\Delta C(t)$, has been created with a time constant that is characteristic of the traps which have released their trapped charges and has the form

$$\Delta C = C_2 - C(t) = \Delta C(t=0)\exp\left\{\frac{-t}{\tau_e}\right\}, \tag{3.6}$$

with the time constant τ_e given by

$$\tau_e = \left(e_h\right)^{-1}, \tag{3.7}$$

where e_h is the rate of hole emission from the trap, which, through the principle of detailed balance, is given by

$$e_h = \sigma_h v_{th} N_v \exp\left\{\frac{-\left(E_{tr} - E_v\right)}{kT}\right\}, \tag{3.8}$$

with σ_h being the hole capture cross-section of the trap, v_{th} is the mean velocity of valence band holes, and N_v is the density of hole states in the valence band. For semiconductors, v_{th} and N_v are proportional to $T^{1/2}$ and $T^{3/2}$, respectively. Thus, an Arrhenius plot of ln (T^2/e_h) vs. $1/kT$ is expected to be a straight line with a slope equal to $(E_{tr}-E_v)$ and an intercept proportional to σ_n. Setting E_v to zero, as is usual, then the slope is simply the trap activation energy, E_{tr}, provided that the concentration of traps is small with respect to N_A, the trap concentration is given by

$$N_{tr} = 2N_A \frac{\Delta C(t=0)}{C_2}. \tag{3.9}$$

Lang also developed a neat graphical tool for looking at where a deep level defect may be. This graphical technique, illustrated in Figure 3.3, is known as the "rate window" plot and is a plot of ΔC vs. T. As the temperature increases, the DLTS experiment begins to enter the region where there is enough thermal energy to excite the trapped carriers out from the traps. This is the area marked "a" in Figure 3.3. At first, the change in capacitance is small, area "b" in Figure 3.3, as only a few carriers escape. With increasing temperature, the change in capacitance increases as more carriers are thermally freed from their traps, area "c" in Figure 3.3. However, with still increasing temperature, there is a competing effect. The traps are still capturing carriers, but carriers now have enough thermal energy to easily escape the trap. Thus, the total available

capacitance change is decreased due to the lack of trapped carriers in that temperature range, which is area "d" in Figure 3.3. This entire process can repeat itself throughout the temperature range as shown in area "e" of Figure 3.3.

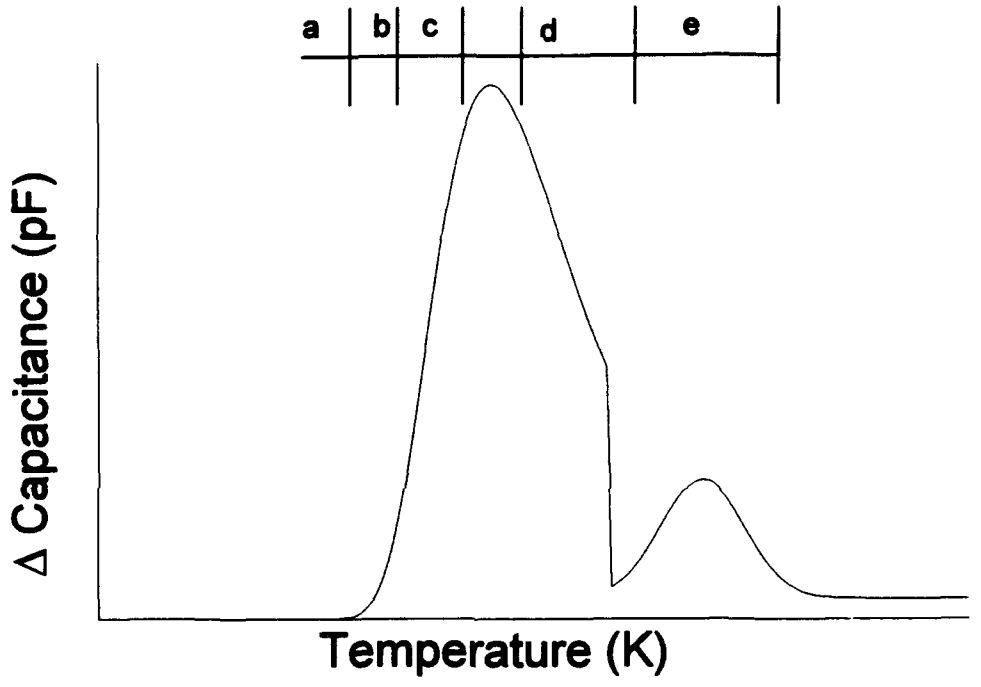

Figure 3.3. Rate window plot example.

Rate window plots contain a great deal of information. Equation 3.9 relates the peak height of a transient in a rate window plot to the trap concentration. Also, the approximate location of the trap, temperature wise, can be easily spotted as the temperature at which the rate window plot peaks. In the rate window plot, peaks that are relatively narrow denote traps that are very well defined in their activation energy. These traps are

very closely centered, in energy, around the activation energy gleaned from the Arrhenius plot. Conversely, broad peaks denote traps whose average energy is that from the Arrhenius plot, but in actuality, may have a large distribution of activation energies. Extremely broad peaks may also be a sum of several, smaller, less distinct peaks. However, it is unlikely that the fitting program to be discussed in Section 3.4 Method of Data Analysis will provide a definitive time constant due to the multiple overlapping transients. Thus, these broad peaks will likely yield no information other than there are deep level defects there.

3.3 DLTS Equipment and Procedures

The DLTS equipment setup is shown in Figure 3.4. The sample is mounted in a brass cold head inside the sample chamber. Good thermal contact exists between the diode canister and the cold head. Temperature measurements are made by a Fe:Pt sensor which is in thermal contact with the cold head. The entire chamber is maintained under a vacuum during the measurements to prevent ice buildup in the chamber. Ice interferes with the sensors and could damage the system including the diodes being measured. The pulse generator and Sula Technologies capacitance meter are mounted in the same sub-rack. The analog signal from the capacitance meter is converted by an A/D—D/A board inside the PC.

Bias and pulse setting made in the program on the PC are converted to analog by the same A/D—D/A board. Temperature control is provided via an IEEE-488 bus between the PC and the Temperature controller. All

control functions are integrated into a graphical program built by Capt Dan Johnstone in Lab Windows. Pulse bias and measure bias are determined by first taking CV measurements at room temperature and 100 K. From these measurements, the behavior of the diode depletion width with respect to temperature can be determined. The primary focus is to ensure the depletion width is reasonably far away from the n^+—p junction interface in order to avoid possible sheet effects at the junction interface. Second, a wide depletion width combined with the fixed diode cross-section, leads to a greater possible capacitance change due to the larger number of possible traps contained in the depletion width. However, there is a breakdown electric field associated with this operation. While the exact breakdown for $GaInP_2$ is not known, GaAs can be used as a guide where the electric field associated with either forward or reverse bias should be less than 1.0×10^5 V/cm. The important item to remember is that the applied bias is not the only voltage present and there is a built-in potential associated with the n^+—p junction. The net voltage is given by $V_T=V_{bi} - V_{bias}$.

Once the bias voltages are set, there is the problem of pulse length and the measure delay. The measure delay is the time between any two capacitance measurements. The system can not measure one capacitance transient all at once. It pulses the bias voltage many times, taking capacitance measurements over these transients. Each measurement is made up of two measurements taken with some delay time. From this, the capacitance transient measurement is built. Since these two times are

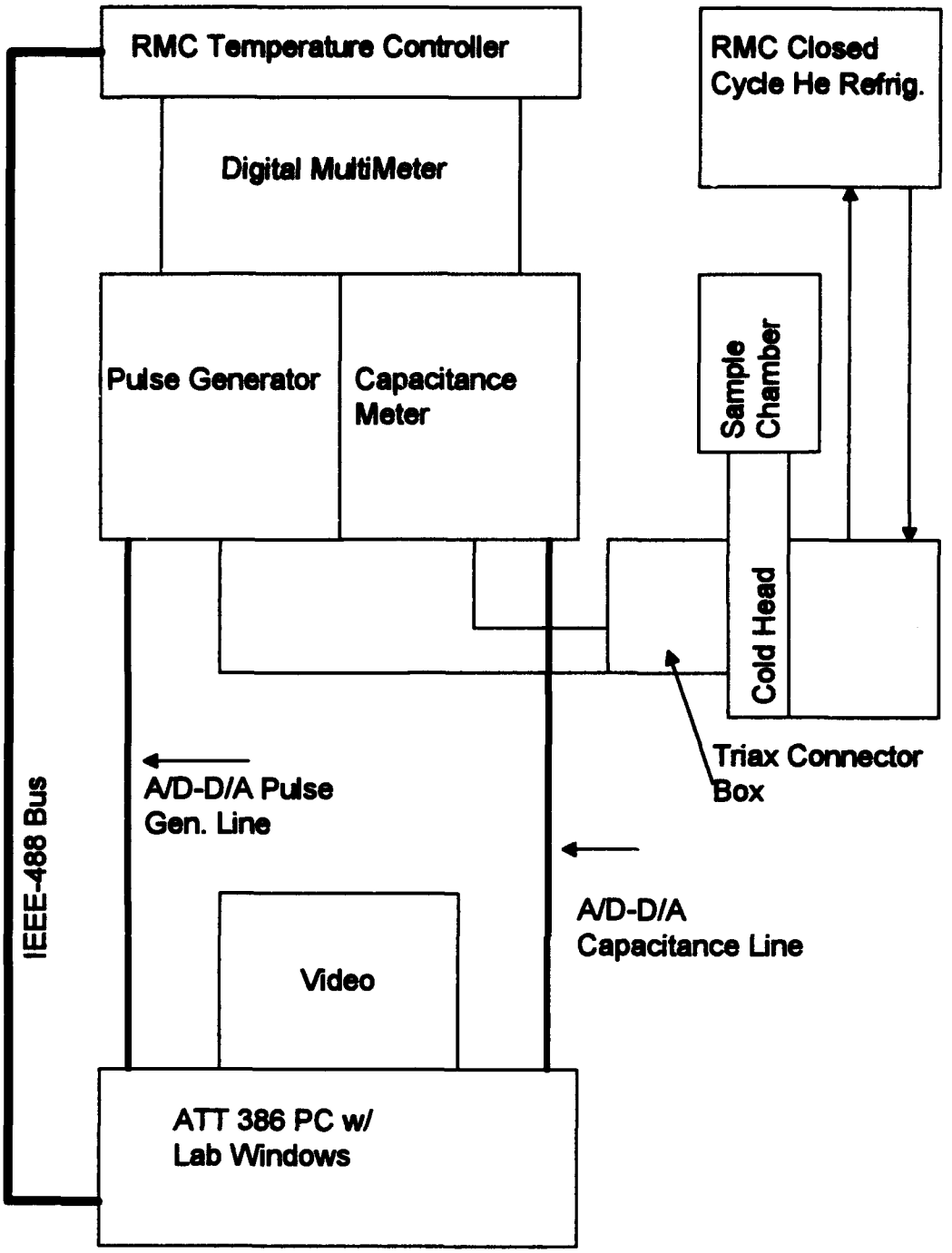

Figure 3.4. DLTS equipment schematic.

dependent on the time constant of the trap, which is unknown at this point, pure trial and error was used to find the best times. Some time combinations are disallowed by the software or the physical limitations of the equipment. After setting all these parameters, there are two left, the number of transients to be averaged and the temperature range and increment. Again, through trial and error, we determined that 200 was the optimum number of transients to average. This balanced the total time it takes to build the transient and the inherent system noise that can hide a single transient. The temperature parameters, for the first run at least, were set to gather data from 20 to 550 K in steps of 5 K. After the first run, a rate window plot could be made and the search range narrowed to eliminate those temperature ranges where no traps were thermally excited. The temperature controller itself has three parameters to set: Integral, Rate and Gain. The optimum numbers here were determined to be 1,0,1020 for $T > 250$ K and 10,20,1020 for $T < 250$ K. The setting of these parameters is based solely on observation of the behavior of the cold head temperature and the temperature controller during a temperature change. Settings other than these can lead to a wildly oscillating temperature of the cold head that takes several tens of minutes to settle to the target temperature, if it settles at all. The settings listed above lead to smooth temperature transitions with settle times of less than 90 seconds.

3.4 Method of Data Analysis

The result of a data acquisition run is an ASCII data file. This file contains, for each temperature data was sampled at, a two line header

made up of temperature, bias and time scale and interval between data points followed by 1024 data points that contains the transient. The first step in the analysis is a QBasic program that I wrote which generates a data file containing four columns: Temperature, Low Capacitance, High Capacitance and Δ Capacitance. This file is used to generate rate window plots and capacitance vs. temperature plots. Next, the file is downloaded from the DLTS computer and transferred to the local Sun SPARCstation network at AFIT. It is here that the actual analysis takes place. A program derived from *Numerical Recipes* (Press:1989) fits one, two or three exponentials of the form

$$C(t) = C_0 \exp\left\{\frac{-\tau_e}{t}\right\}, \tag{3.10}$$

where τ_e is the parameter of interest, the time constant governing the decay. Each transient contained in the data file is fitted and an $(1-r^2)$ error tolerance assigned to it. Another data file is generated that contains the temperature of the data point, the fitted time constant and the error tolerance and a number indicating that it is the first, second or third exponential fit. A second program takes the output from this one, asks for an error tolerance, and produces an output file containing the information for the Arrhenius plot. These files are then downloaded and analyzed for a linear fit using TableCurve by Jandel Scientific. If there is a trap present, some part of the graph of the Arrhenius plot of ln (T^2/e_h) vs. $1/kT$ will be linear and the slope is the trap activation energy.

4. Sample Growth and Preparation

All of the samples used in this study were grown by RTI, Research Triangle, NC using the Metal Organic Chemical Vapor Deposition (MOCVD), which is discussed in Section 4.1. Once they were delivered, the samples had to be processed into diodes, as explained in Section 4.2.

4.1 Metal Organic Chemical Vapor Deposition (MOCVD)

The basic idea behind MOCVD is to use flowing organic gasses as carriers for the compounds wanted in the semiconductor.(Böer:1992) The substrate, GaAs for $GaInP_2$, is placed in a vacuum chamber which is then evacuated. Once this is achieved, the sample and the chamber are then heated to the target temperature, usually between 700 and 900 K. The gasses are then forced over the substrate through convection, and diffusion carries the target compounds to the boundary layer where the building of the structure takes place. The exact processes and governing rate equations are not well known yet.(Böer:1992)

Using MOCVD, the structure in Figure 4.1 was grown for processing into diodes for DLTS measurements. First, a 3 μm layer of p—type $GaInP_2$ was grown to form the base of the p—n junction. For this study, the acceptor dopant is zinc and two levels of acceptor doping are available, $N_A = 5.0\times10^{16}\,cm^{-3}$ and $N_A = 1.2\times10^{17}\,cm^{-3}$. Next, a 0.3 mm layer of n^+—type $GaInP_2$ was grown as the other side of the p—n junction. This layer was grown as n^+ in order to ensure the depletion width under reverse bias conditions existed in the p—type $GaInP_2$ layer. Under this condition,

the trap information found using DLTS is for the p—type $GaInP_2$. Finally, a 0.3 mm layer of n^+—type GaAs was grown as a cap layer. GaAs was used for the cap in order to achieve good ohmic contacts which are very difficult to achieve with $GaInP_2$.

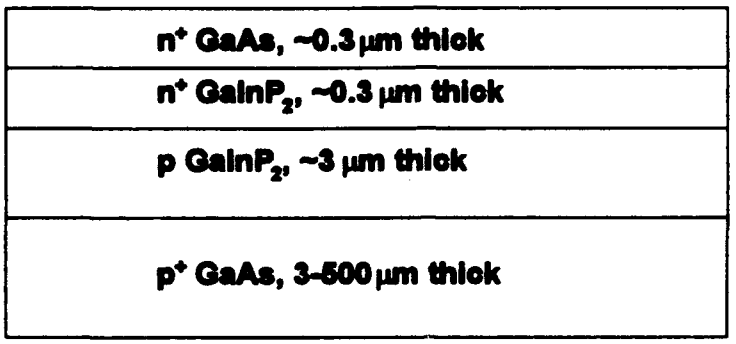

Figure 4.1. n^+—p $GaInP_2$ structure for diodes.

4.2 Mesa Diode Processing

Once the semiconductor material was received, it needed to be processed into mesa diodes. All of this work was performed by Kitt Reinhardt. The first step was to sputter Ti onto the GaAs cap layer to improve the metal to semiconductor bonding of the Au contact layer sputtered on top. Each of these layers is approximately 300 angstroms in thickness. Each 1 inch x 1 inch wafer was then covered in photoresist material and masked. The areas of photoresist exposed to the light through the mask were chemically changed so that they could not resist the etch in the next step. In the etching, two different etch formulas were used. $NH_3OH:H_2O_2:H_2O$, in a ratio of 2:1:10, was used to etch GaAs 100× faster

than $GaInP_2$. Likewise, $HCl:H_2O$, in a ratio of 1:20, was used to etch $GaInP_2$ 100× faster than GaAs. Each wafer was etched down to the p^+ GaAs substrate. Figure 4.2 shows the resulting mesa diode.

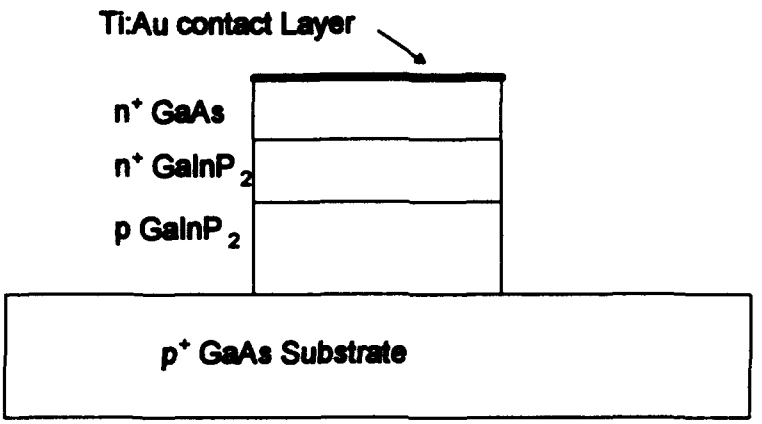

Figure 4.2. n^+—p Mesa diode structure.

The resulting diodes were cut into square sets of four and "canned". In being canned, each of the diode sets were bonded to a four or twelve pin canister. This bond is electrically conductive so the diode is grounded to both the ground pin and the canister. Each of the four diodes, in the case of the twelve pin canister, were wired to a pin on the canister. In the case of the four pin canister, only three diodes could be wired since the fourth pin was taken by the ground.

5. Results and Discussion

The n^+—p $GaInP_2$ junction diodes used in this study are listed in Table 5.1. This matrix shows the number of diodes in each category that were available and how many returned the data presented in this chapter. All the irradiated diodes were exposed to the same 1×10^{16} cm^{-2} fluence of 1 MeV electrons. A complete presentation and discussion follows.

p—Doping Density (cm^{-3})	Irradiated	Number Tested	Number Returned Data
5.0×10^{16}	No	16	1
5.0×10^{16}	Yes	4	1
1.2×10^{17}	No	8	1
1.2×10^{17}	Yes	5	1

Table 5.1. $GaInP_2$ n^+—p junction diodes used in this study.

5.1 Rate Window Plots

Contained within the DLTS data file are two very important relationships other than the activation energy. The first is the change in capacitance (ΔC) within a transient with respect to temperature. This is the rate window plot discussed in Section 3.4. Peaks in this plot denote the presence of deep level defects. The width of the peak may also give some insight as to if there is one distinct defect, or a large number of defects. Narrow peaks translate to one distinct peak with a well defined activation

energy. Wide peaks are translate to a large number of defects whose average activation energy is the DLTS result. Figures 5.1 and 5.2 present the rate window plots for the diodes which returned data.

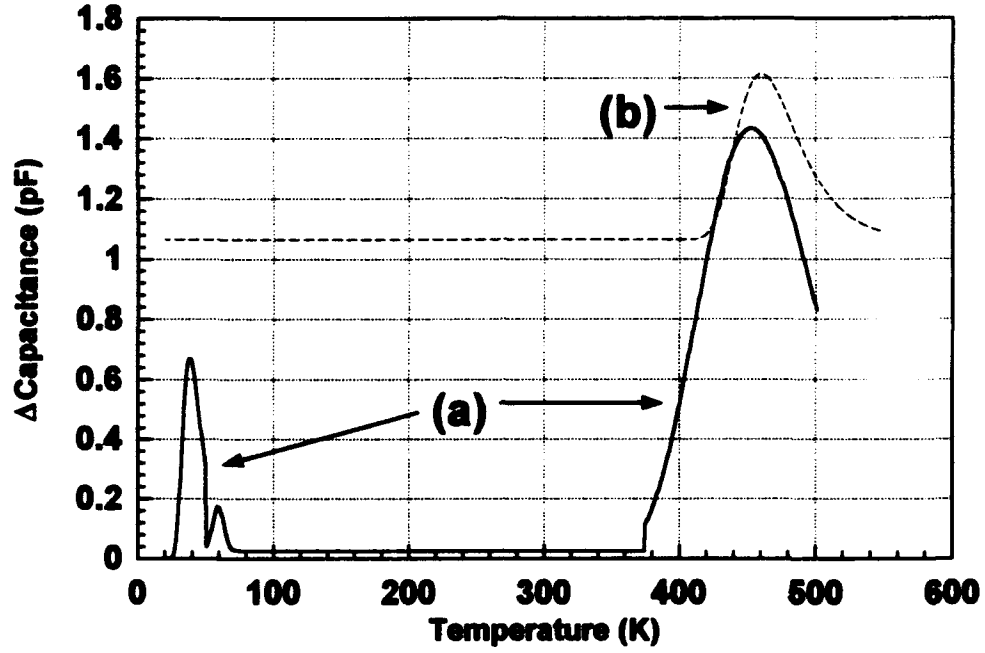

Figure 5.1. Rate window plot for $N_A = 5.0\times10^{16}$ cm^{-3}. Figure (a) is for the unirradiated diode, Figure (b) is for the irradiated diode where ΔCapacitance has been multiplied by 15 in order to present it on the same scale as Figure (a).

Figure 5.1 presents the rate window plot for the low doped, $N_A = 5.0\times10^{16}$ cm^{-3}, diode, including data for the unirradiated diode, figure(a), and data for the irradiated diode, Figure (b). For the unirradiated diode, Figure 5.1(a) clearly shows three traps. The first trap from the left is a minority carrier trap. This is known from reconstructing the shape of the transients in this temperature range. A minority carrier

trap transient starts with a high capacitance and decays to a low capacitance, which is the case for the first trap. The other two traps are majority carrier traps. For the irradiated diode, Figure 5.1(b) shows only one trap. The data plotted here, that irradiation changes the semiconductor to produce only one dominant trap, has been seen before, in InP (Messenger:1992), and is consistent with that work.

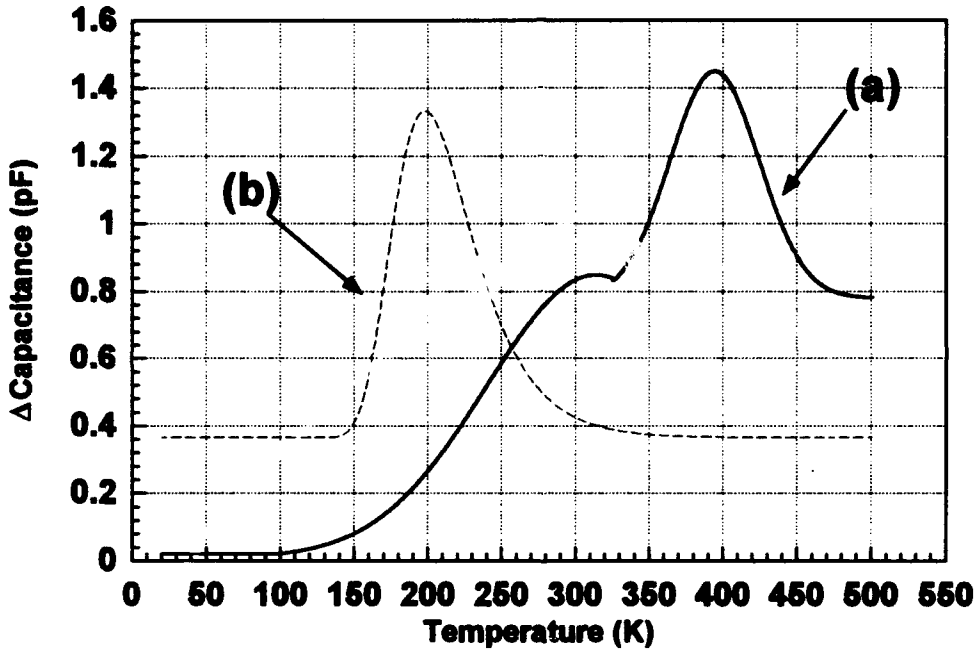

Figure 5.2. Rate window plot for $N_A = 1.2\times10^{17}$ cm^{-3}. Figure (a) is for the unirradiated diode, Figure (b) is for the irradiated diode where ΔCapacitance has been multiplied by 10 in order to present it on the same scale as Figure (a).

The same trends seen in Figure 5.1 are clearly present in Figure 5.2. For the unirradiated diode, multiple traps are present, in fact, there are two in this case. After irradiation by 1 MeV electrons, with a fluence of

1.0×10^{16} cm^{-2}, only one dominant trap is detectable by the DLTS method. This is consistent with Messenger's 1992 InP paper.

5.2 Capacitance vs. Temperature Plots

Contained in the same file as with the ΔCapacitance vs. Temperature data is the Capacitance vs. Temperature data. In general, a plot of Capacitance vs. Temperature should show only a trend of increasing capacitance with increasing temperature. However, in the case of the unirradiated diode doped at $N_A = 1.2\times10^{17}$ cm^{-3}, a discrete step occurs around 150 K. Figure 5.3 presents this data.

Clearly, Figure 5.3 shows a strong temperature dependence of capacitance for this diode. In order to better understand what occurred here, a plot of Built-in Potential vs. Temperature and Depletion Width vs. Temperature was constructed. This data was taken using a capacitance vs. voltage program written by Capt Dan Johnstone. Based upon a diode's physical characteristics, size and relative dielectric constant, the program measures capacitance vs. voltage and then computes the built-in potential and depletion width vs. voltage. By taking these measurements over a given temperature range, a plot of built-in potential vs. temperature and depletion width vs. temperature for a fixed voltage can be constructed. This information presented in Figure 5.4.

Clearly, the same temperature dependence at 150 K is evidenced in Figure 5.4 as in Figure 5.3. The "steps" visible in Figures 5.3 and 5.4 are due to the existence of an electron state in the band gap situated in a

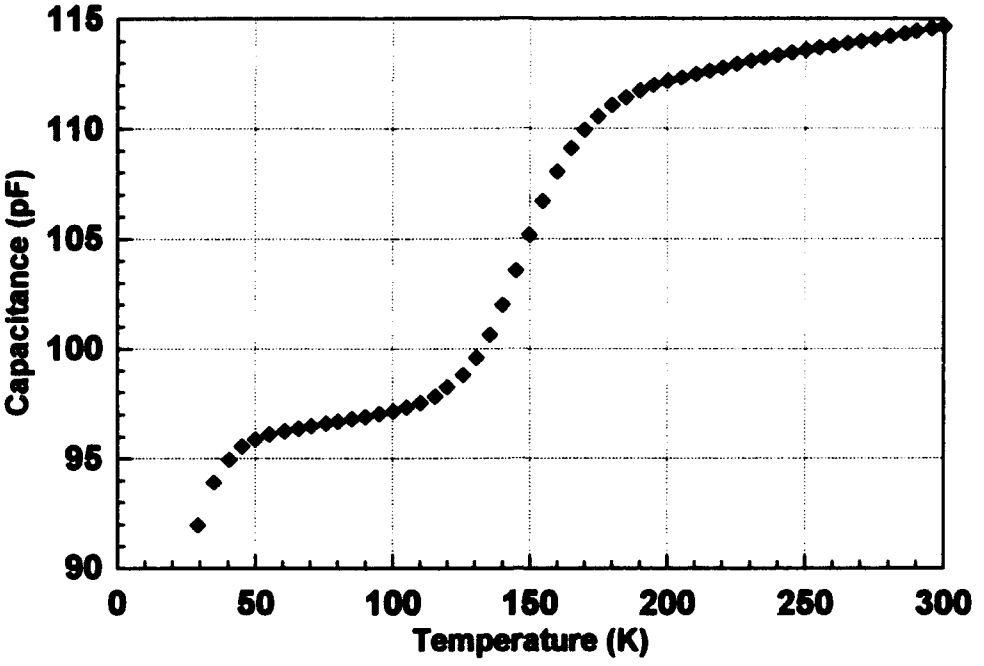

Figure 5.3. Capacitance vs. Temperature for an unirradiated diode with $N_A = 1.2\times10^{17}$ cm^{-3}.

particular way. The energy of this state is such that as the semiconductor's temperature nears 150 K, one of three models begins to occur. If this state is due to a donor impurity, its valence electron, or electrons, has sufficient thermal energy to transition into the conduction band. If this state is due to an acceptor impurity or a majority carrier trap, a hole trap in p—type material, electrons in the valence band have enough thermal energy to transition into the acceptor state or the trap, in either model, the effect is a hole emitted into the valence band. The net effect is a change in the total charge in the depletion region with corresponding changes in the depletion width, the total capacitance and the built-in potential as evidenced in

Figures 5.3 and 5.4. It is not clear, however, which of the three models presented has taken place in this diode.

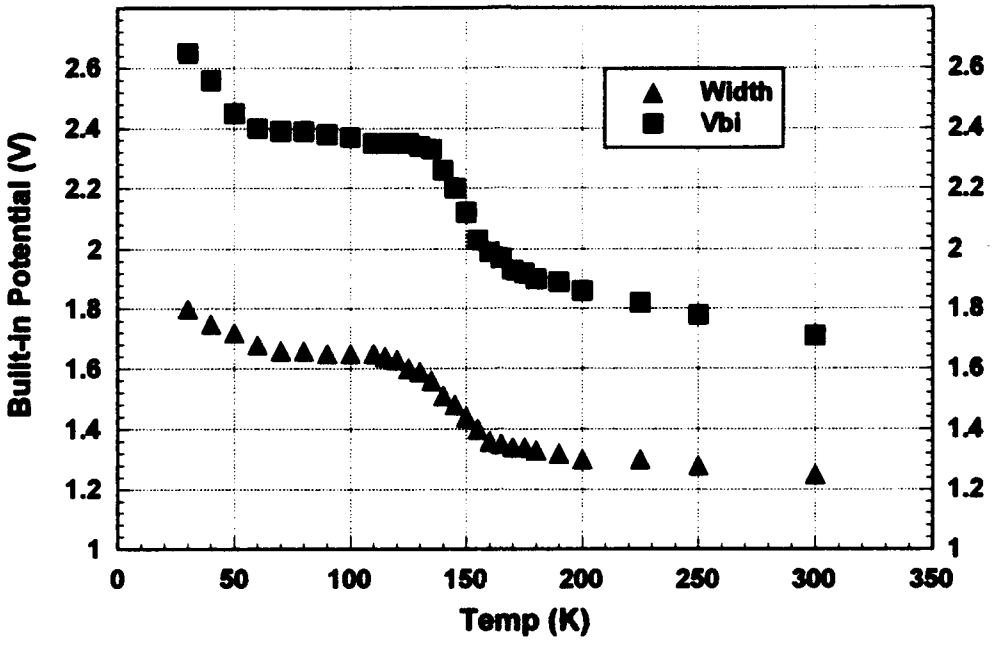

Figure 5.4. Built-in Potential and Depletion Width vs. Temperature for an unirradiated diode with $N_A = 1.2\times10^{17}$ cm^{-3}, with $V_{bias}=-1.0$ V.

5.3. Deep Levels in $GaInP_2$

In $GaInP_2$, it is thought that deep level defects dominate the dark current in n^+—p junction diodes. (Reinhardt:1992) The solar cells proposed (Cavicchi:1991) will utilize the n^+—p $GaInP_2$ junction diodes studied here. Using DLTS, it is possible to find the activation energy, concentration and capture cross-section of these deep level defects within

certain limitations. In Section 3.2, a method for determining the activation energy of a deep center was presented. The four distinct categories of diodes looked at for this study are listed in Table 5.1. The two definitive parameters are the acceptor concentration and the amount of 1 MeV electron irradiation each received. The criterion for judging if a diode "returned data", as listed in Table 5.1, was quite simple. If the arrhenius plot of the data contained a clear trap activation energy, with a clear trap activation energy defined as a linear trend of more than four data points, then the diode "returned data".

Of great importance is the repeatability of these measurements. It is well known that defects in semiconductors can be annealed out at room temperature and above. (Reinhardt:1992) In conducting this research, the DLTS data acquisition temperature range was 20 to 550 K and taken over a period of 8 to 12 hours. Clearly, annealing will take place. This annealing will, most likely, prevent repeating these data runs and duplicating the exact results due to changes in the semiconductor structure.

There are two trends that can clearly be seen in Figures 5.5 and 5.6. First, for a fixed acceptor concentration, the effect of the electron irradiation is to lessen the activation energy of the defect, i.e., the trap becomes more shallow and closer to the valence band. Electron irradiation changes the location of the constituent atoms in the semiconductor which changes the crystalline field.

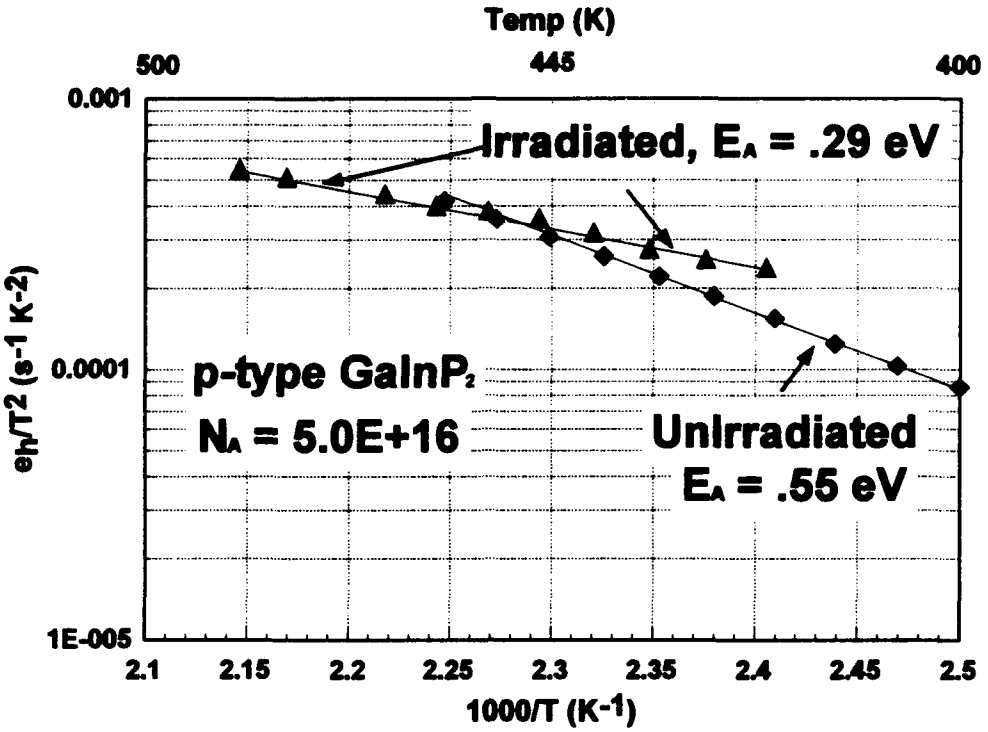

Figure 5.5. DLTS data arrhenius plot for $N_A = 5.0\times10^{16}$ cm^{-3}.

The exact mechanism of interaction between the deep level defect and the electron irradiation induced changes is not well quantified. Secondly, higher acceptor concentration lowers the unirradiated trap activation energy. This is again due to changes in the semiconductor's crystalline field this time due to substituting impurities into the structure; though, the exact mechanism of interaction between the deep level defect and these changes is not well quantified. The data from Figures 5.5 and 5.6 agrees with trends observed in InP.(Messenger:1992) Table 5.2, in Section 5.4, contains the same data as Figures 5.5 and 5.6.

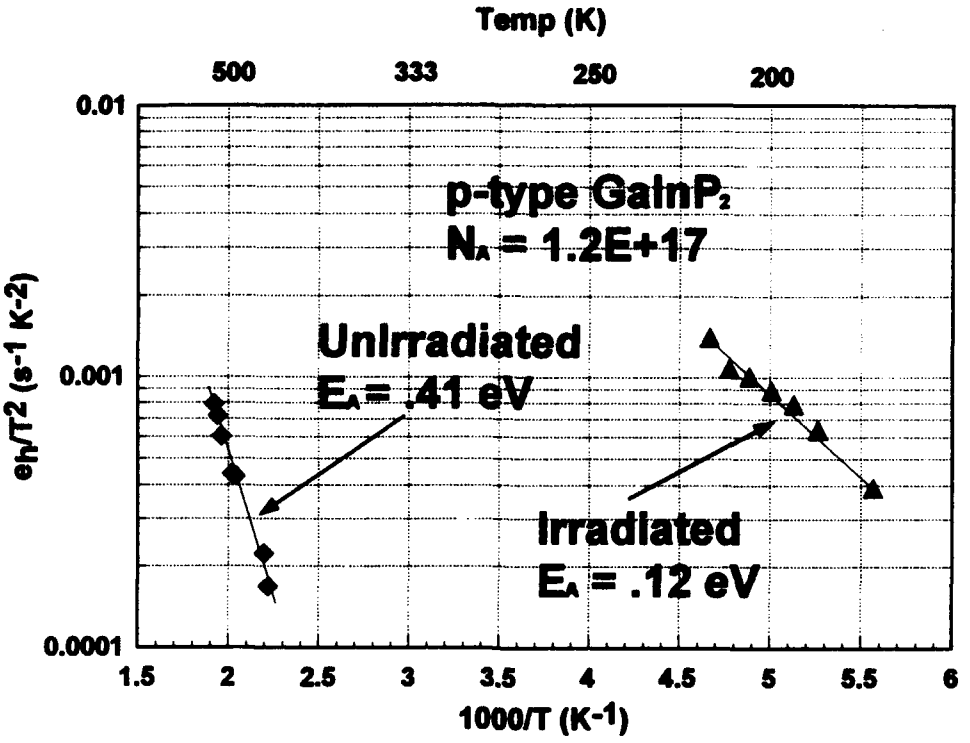

Figure 5.6. DLTS data arrhenius plot for $N_A = 1.2\times10^{17}$ cm^{-3}.

Some DLTS work has been previously done for $GaInP_2$. (Zhu:1990) In that study, $GaInP_2$ was grown by liquid phase epitaxy (LPE) as opposed to MOCVD grown semiconductors used in this study. Two traps were observed with activation energies of 0.39 eV and 0.57 eV. The source of the deep level defects were attributed to vacancies in the phosphorous sub-lattice. It is likely the 0.55 eV trap found in this study is the same as the 0.57 eV found previously.(Zhu:1990) The 0.39 eV trap was not uniquely determined in this study; however, evidence for the deep center can be inferred through the rate window plot, Figure 5.1(a). The first of the majority carrier traps, the second peak from the left, could be the

0.39 eV trap, though a rate window plot is not definitive. The remaining three deep level defects are in $GaInP_2$ semiconductors that have not been previously investigated and the trends can only be compared with work on InP.(Messenger:1992)

5.4. Deep Level Defect Concentration

Also, from information on the rate window plots, deep level defect concentration, N_{tr}, is found. In Section 3.2, Equation 3.9 gives a simple formula for N_{tr} provided $N_A \gg N_{tr}$, which is true for both the irradiated diodes here. Table 5.2 shows the results of this calculation.

N_A (cm^{-3})	Irradiated	Trap (eV)	N_{tr} (cm^{-3})
5.0×10^{16}	No	0.55	1.09×10^{15}
5.0×10^{16}	Yes	0.29	1.35×10^{15}
1.2×10^{17}	No	0.41	2.06×10^{14}
1.2×10^{17}	Yes	0.12	4.74×10^{14}

Table 5.2. Trap Concentration, N_{tr}, for Each Deep Level Defect.

There are two clear trends here. First, for a fixed acceptor concentration, electron irradiation causes a higher trap concentration through the introduction of more defects in the semiconductor structure. However, the sample having higher acceptor concentration has lowered the overall number of traps by an order of magnitude than the sample

having lower acceptor concentration. This is due to changes is the crystalline field caused by the changes induced by substiting acceptor atoms for the normal constituents in the semiconductor structure though the mechanism that leads to lower activation energy is not well quantified.

6. Summary

6.1 Results

Much has been discovered about the traps in p—type $GaInP_2$ that was not previously known. The rate window plots of Section 5.1 show that multiple deep level defects are present in the unirradiated diodes. This agrees with previous work on $GaInP_2$ (Zhu:1990) and InP (Messenger:1992). The effect of electron irradiation, that it changes the semiconductor structure such that there is only one dominant trap, as seen in the rate window plots, Figures 5.1(b) and 5.2(b), is in agreement with work on InP. (Messenger:1992) Though, it is not well understood why only one trap is produced by electron irradiation.

One diode in particular, though it is not clear why only one diode exhibited this behavior, demonstrated a strong dependence of capacitance, built-in potential and depletion width on temperature. Three models for this behavior were proposed. The models are for donor impurities, acceptor impurities and majority carrier trap. It is thought that one of these is present and has a high trap concentration with a sharply defined activation energy such that electrons, at 150 K, have enough thermal energy to transition out of the trap (donor impurity) or into the trap (acceptor impurity and majority carrier trap). In each of the models, the charge characteristics of the depletion region are significantly altered due to the high trap concentration combined with a sharply defined activation energy leading to the corresponding strong temperature dependence as evidenced in Figures 5.3 and 5.4

Deep level defects in $GaInP_2$ are thought to dominate the dark current in n^+—p junction diodes. (Reinhardt:1992) An understanding of the trap activation energies and concentrations is then necessary to understanding dark currents in $GaInP_2$ solar cells. The choice of acceptor concentrations and electron irradiation shown in Table 6.1 is based upon the need to find the most efficient material for the solar cells (acceptor concentration) and its ability to withstand the space environment (1 MeV electron irradiation). Two trends in the results were noted and discussed in Section 5.4. For a fixed acceptor concentration, electron irradiation acts to lower the trap activation energy. Secondly, a higher initial acceptor concentration also leads to lower trap activation energy. While the mechanisms for this are not well quantified, the trends evidenced here are in agreement with previous work on InP. (Messenger:1992) Some DLTS work has been previously performed on $GaInP_2$. (Zhu:1990) The 0.55 eV trap shown in Table 6.1 is most like the 0.57 eV trap reported by Zhu. Evidence exists in the rate window plot, Figure 5.1(a), for the 0.39 eV trap reported by Zhu but not uniquely determined here. The remaining three $GaInP_2$ samples used in this study have not been previously studied; though, the trends observed agree with previous work on InP. (Messenger:1992) The trap concentration, N_{tr}, is also reported in Table 6.1. The equation for trap concentration is Equation 3.9. Two trends are noted here. First, irradiation produces a higher trap concentration through the introduction of more defects in the semiconductor structure. Second, a higher acceptor

concentration leads to lower trap concentration though the mechanism is not well quantified.

$N_A(cm^{-3})$	Irradiated	Trap (eV)	$N_{tf}(cm^{-3})$
5.0×10^{16}	No	0.55	1.09×10^{15}
5.0×10^{16}	Yes	0.29	1.35×10^{15}
1.2×10^{17}	No	0.41	2.06×10^{14}
1.2×10^{17}	Yes	0.11	4.74×10^{14}

Table 6.1. DLTS data for $GaInP_2$.

6.2 Recommendations

While much has been accomplished in understanding the basic electronic properties of $GaInP_2$, this thesis is only the beginning. The Hall Effect measurements still need to be completed. The work on the $GaInP_2$ n^+—p junction diode has only begun. The initial numbers reported here will, in time, be further enhanced by more DLTS profiles of similar diodes and there remains a highly doped, $N_A = 2.0\times10^{17}\ cm^{-3}$, diode to investigate. Most, if not all, of this work is already slated for completion as part of Kitt Reinhardt's dissertation.

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The $GaInP_2$ n^+-p junction diode has recently become important to the development of high efficiency $GaInP_2$ /GaAs dual junction solar cells, which have a demonstrated air mass 1.5 conversion efficiencies in excess of 27%. In order to study the effects of long term exposure to the space environment, the $GaInP_2$ n^+-p junction diodes were irradiated with a 1 MeV electron beam with a fluence of 10^{16} electrons/cm^2. Since little is known about deep level defects (traps) in $GaInP_2$, a deep level transient spectroscopy (DLTS) study was made to characterize the traps that are thought to dominate the dark current in $GaInP_2$ solar cells. The measurements indicated that there are a number of majority carrier traps in the p-type base of the $GaInP_2$ n^+-p junction diode. Traps that are identified are located 0.12 to 0.55 eV above the valence band and are attributed to phosphorous vacancies in the lattice..

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