3-2022

Simultaneous Actuation and Sensing of Electrostatic MEMS

Jacob E. Song

SIMULTANEOUS ACTUATION AND SENSING OF ELECTROSTATIC MEMS

THESIS

Jacob E Song, 1st Lieutenant, USAF

AFIT-ENG-MS-22-M-063

DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY

AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

AFIT-ENG-MS-22-M-063

SIMULTANEOUS ACTUATION AND SENSING OF ELECTROSTATIC MEMS

THESIS

Presented to the Faculty

Department of Electrical and Computer Engineering

Graduate School of Engineering and Management

Air Force Institute of Technology

Air University

Air Education and Training Command

in Partial Fulfillment of the Requirements for the

Degree of Master of Science in Electrical Engineering

Jacob E Song, B.S.E.E.

1st Lieutenant, USAF

March 24, 2022

AFIT-ENG-MS-22-M-063

SIMULTANEOUS ACTUATION AND SENSING OF ELECTROSTATIC MEMS

THESIS

Jacob E Song, B.S.E.E.
1st Lieutenant, USAF

Committee Membership:

Matthew J Vincie, Ph.D
Chair

Hengky Chandrahalim, Ph.D
Member

James M Sattler, Ph.D
Member

AFIT-ENG-MS-22-M-063

Abstract

Micro-Electro-Mechanical Systems (MEMS) are devices that play important roles of sensing and actuation in many different industries including automation, electronics, medical, communications, and defense. In order to make full use of these devices, it is important to understand the peripherals that enable these devices. Simultaneous actuation and control of MEMS is an important area of research as it enables feedback control of these devices and allow them to maintain performance as they depreciate over their lifetime. The aim of this thesis is to perform a design space analysis on an electrostatic MEMS simultaneous actuation and sensing circuit that is driven by a Pulse Width Modulated (PWM) signal and sensed by a capacitor divider interface circuit. A new variant to the capacitor divider interface is discussed and takes advantage of the leakage problem associated with this circuit. Furthermore, the important design variables and their impacts are investigated. The results found herein are generalized and may be applied to any electrostatic MEMS.

Table of Contents

Page

List of Figures

List of Tables

List of Abbreviations

SIMULTANEOUS ACTUATION AND SENSING OF ELECTROSTATIC MEMS

I. Introduction

1.1 Motivation

In the Air Force, MEMS technology has enabled numerous technologies such as lasers, RF devices, sensors, data storage, and aircraft control. As MEMS is still a relatively new field, advances in research are being made in all areas of MEMS including its supporting technologies. One such area of interest is the simultaneous control and sensing of electrostatic MEMS. This research explores the combination of a PWM drive signal and capacitive interface circuit as the foundation of a simultaneous control and sensing system for such devices. A simultaneous control and sensing system is important because it allows for closed loop feedback of actuators. This prevents the loss of control over time as the device wears down because the position of a device is constantly measured. In general, feedback systems are more reliable, robust, and stable compared to open loop systems. Another advantage of a PWM drive signal to perform capacitive actuation and sensing with a single signal. As PWM circuits can be implemented solely with timing it is a cheaper alternative to analog DC drive circuitry, which requires high-voltage linear amplification to actuate many types of electrostatic MEMS. Linear amplification is normally very inefficient, especially when high-voltage output is required. To increase efficiency, the amplifier circuitry increases in size and complexity, which drives up cost. Furthermore, such amplifiers primarily are confined to low frequency (<100 MHz) applications. The capacitor divider interface circuit is a simple circuit that measures changes in capacitance through

the modulation of the amplitude of a PWM signal. This simplicity allows for easy and cheap integration and the modulated amplitude of the PWM signal is used to measure the position of the MEMS device. On the other hand, traditional charge-to-voltage converters measure the change in capacitance by the change in charge stored on the MEMS, this circuit often suffers from low sensitivity, small magnitude, and voltage drift. Overall, the proposed system can be used in many defense areas such as munition guidance, surveillance, embedded sensors, microrobotics, and, aircraft control.

1.2 Research Goal

The overarching goal of this research is obtain an experimentally validated design of and design space analysis on a simultaneous actuation and capacitive sensing circuit that is driven by a PWM signal and has a capacitor divider as its interface circuit. The design space analysis conducted will identify and describe the effects of the important design variables of the system that are needed to shape the circuit for any specific electrostatic MEMS device or application.

1.3 Research Objectives

In order to achieve the goal, the research objectives for this thesis are to design, test, and evaluate the proposed system.

1. Identify the important factors that need to be considered when designing the proposed system.

2. Design, simulate, and experimentally validate the circuit designs of the proposed system.

3. Compare the performance of the high pass variant of the capacitor divider circuit to the traditional capacitor divider circuit in order to see if the high pass variant is a viable solution.

4. Compare amplitude modulation and amplitude integration analog signal processing schemes on capacitance estimation in order to determine the differences between them.

1.4 Document Overview

In this document, chapter II will discuss background information on MEMS technology and interface circuits particularly focused on electrostatic MEMS. Chapter III will describe the steps conducted when building the system to actuate and control electrostatic MEMS device. Chapter IV will describe analysis of the results. Chapter V will describe the conclusion reached in this research thesis and future work.

II. Background and Literature Review

How does a cellphone know what orientation it currently is in? Phones have a very small microelectronics that can sense the orientation due to gravity and send that information to the phones processor. This is one of countless examples of how microelectronics are prevalent in present day society. As seen in figure 1, since the 1990's rapid research and development has allowed microelectronics to grow into a 20 billion dollar industry and overtake their larger electronic counterparts and even continue to find itself in more and more areas. Despite having 50 years of research, microelectronics are still heavily researched today. In 2020, microelectronics displaced hypersonics as Deparment of Defense's number one technology priority [2]. One major subdomain of microelectronics is the area of MEMS. MEMS are systems that combine electrical and mechanical components into small units ranging in size from micrometers to millimeters [3]. These systems operate by transducing energy from the

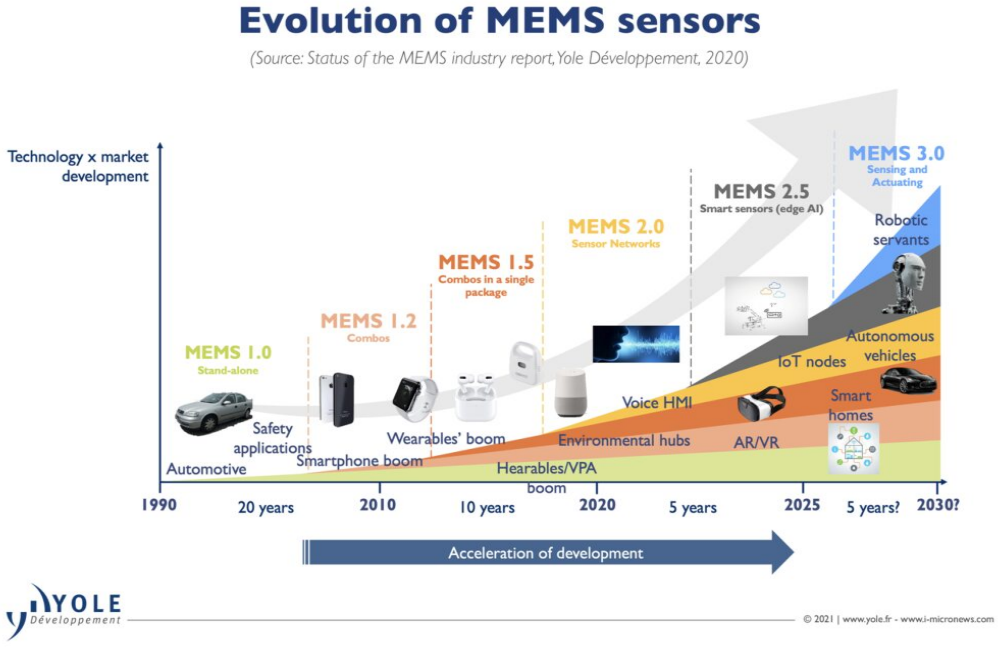


Figure 1: Evolution of MEMS technology in the consumer market space [1].

electrical domain into other physical domains or vice versa. As in the earlier phone example, the MEMS is transducing the forces of gravity into an electrical signal that the phones processors can read. The physical domains include but are not limited to chemical, electrical, optical, RF, mechanical, acoustic, biological, and atmospheric domains.

MEMS are popular today because they offer numerous benefits. MEMS are low energy, inexpensive, small, efficient, have improved sensitivity, accuracy and reliability, low power, easy to integrate, reproducible, and provide parallelism in operation. [4] Consequently, MEMS can be distinguished into 6 different categories: sensors, actuators, RF MEMS, optical MEMS, microfluidic MEMS, and Bio MEMS [3, 5, 6, 7, 8, 9, 8]. Due to this variety of use, MEMS have exploded into every aspect of everyday life. As seen in Figure 2, they play a huge role in a variety of industries. Some of note are the automotive industry, consumer electronics, industrial application, communications, defense/military, medical, biomedical, microfluidics, biotechnology and many more [3, 5, 4, 6, 10, 11, 12, 13].

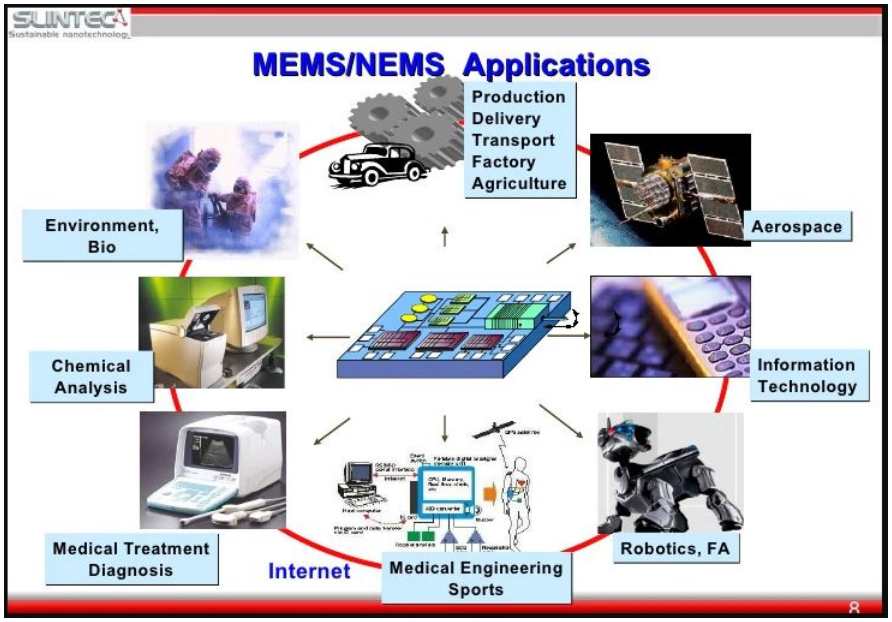


Figure 2: A few examples of MEMS applications [14].

2.1 Electrostatic MEMS

Of all the different types of MEMS, electrostatic or capacitive MEMS are one of the more popular devices today. They are used in devices that need to be inexpensive, low power, and small in size such as gyroscopes, accelerometers, fluid level detectors, strain and pressure sensors, etc.[3]. Capacitive MEMS are often chosen rather than their alternatives due to their robustness and compatibility with existing integrated circuit fabrication technology, without losing out on performance [3]. An electrostatic MEMS can be described simply as two isolated conductors coupled by an electrostatic force. The two conductors create a capacitor based on the geometry and dielectric between the conductors. Capacitance can vary in an electrostatic MEMS in two ways. First, one conductor is fixed while the other conductor is mobile where the electric force generated by a voltage difference across the capacitor pulls the mobile side towards the fixed side. The change in displacement causes a detectable change in capacitance. A general model is depicted in Figure 3, where the mobile side is modelled by a spring. The second way to change capacitance is to change the dielectric constant between the conductors. This can occur by changes in the chemical composition of the fluid between the plates. This simplicity of design and handling has made electrostatic MEMS a popular choice to be used as actuators or sensors.

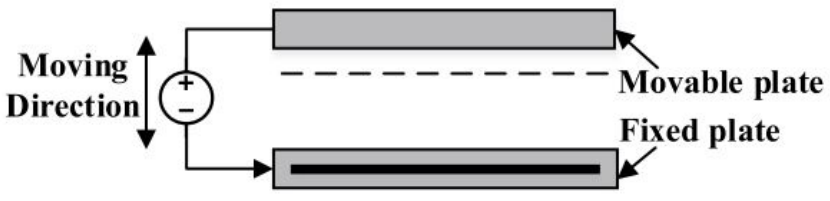


Figure 3: Mechanics of a basic electrostatic actuator [15].

2.2 Electrostatic Actuators and Sensors

When designing a MEMS, electrostatic MEMS actuators are generally considered first as the mechanism to actuate MEMS because of their simple design, ease of fabrication and low power consumption [16]. Another advantage of electrostatic MEMS is that the same device can be used as a sensor or actuator. As mentioned earlier, electrostatic MEMS actuators use the electrostatic force to pull a mobile conductor towards the fixed conductor as seen in Figure 3. According to Coulombs law, when a voltage is applied across two plates the charges on both plates generate a force that is inversely proportional to the distance between the plates. The electrostatic force, F_E, and external force, F_{EXT} are balanced by the spring force, F_K, that tries to keep the mobile plate in place at an unperturbed location.

$$\sum F = F_E + F_K + F_{EXT} = 0 \tag{1}$$

Changing the voltage will cause an imbalance between the two forces, so the movable plate has to move closer or farther in order to restore balance. Ideally, the movable plate would have a range limited only by the initial gap between the two plates. However, that is not the case because of the instability between the spring and electrostatic forces. During actuation, the electrostatic force increases faster than the spring force and as a result at 1/3 the distance of the initial gap, the mobile conductor snaps into the fixed conductor causing the device to collapse [17, 18]. This is also known as pull-in instability. This is a well documented issue and much research is being done to increase the displacement range [19]. Other issues with electrostatic actuation are the non-linearity associated with applied voltage and displacement and, depending on the device, the potential requirement of a high voltage actuation signal [16].

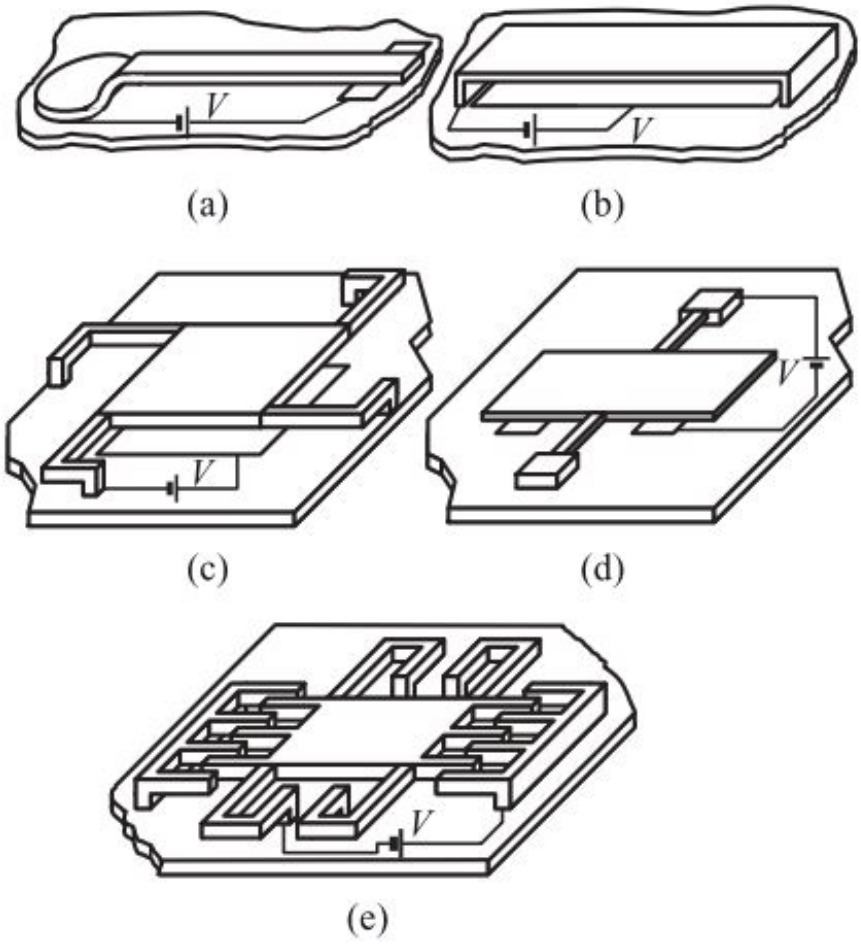


Figure 4: Basic electrostatic MEMS structures [20].

Electrostatic actuators are mainly made in five different configurations: cantilevers (fig. 4a), clamped beams (fig. 4b), parallel plates (fig. 4c), torsional plates(fig. 4d), and combs (fig. 4e). The cantilever design is a cantilever with a parallel plate beneath it. The cantilever can be anchored on one end or if anchored on both ends it becomes a clamped beam. The overlapping area between the parallel plates forms the capacitor. The parallel plate design is very similar. Instead of being anchored on two sides, the suspended plate is anchored at the four corners. The way they operate is very similar to each other. A voltage is applied across the parallel plates and the suspended plate is pulled towards the static plate. These designs only differ in their natural

frequency and mode of vibration. Another design is the torsional actuator. The torsional actuator is similar to the parallel plate actuator, but it is suspended along the mid line of the parallel plates as seen in fig. 4d. The two pads provide the force necessary to cause rotational actuation about the axis of the arms. The previous four designs have motion that is mostly in the vertical direction. The last design is the comb drive design as shown in fig. 4e. This design consists of two interdigitated finger structures, one fixed and one movable. Unlike the other designs, the comb drive moves in the horizontal direction (parallel to surface of the wafer). Usually the heights of the fingers are relatively short (a couple microns). The interdigitated fingers increase the overlapping area which then produces a large overall capacitance. This enables a stronger actuation force to be applied in the horizontal direction. In addition, the electrostatic force generated includes a larger contribution based on the fringing fields at the tips of the fingers. This also eliminates the pull-in effect as the electrostatic force becomes inversely related to displacements instead of the square of the displacement [16]. Comb drive actuators are a popular choice for resonators, electro-mechanical filters, optical shutters, micro-grippers and voltmeters [21].

Electrostatic sensors measure the change of capacitance between the electrodes, where one plate is static and the other is able to move. Electrostatic MEMS sensors have the same exact structures as electrostatic MEMS actuators. However, instead of mechanically responding to an electrical stimulus, they are electrically responding to an external mechanical stimulus by detecting the change in capacitance. Capacitive sensors are one of the most common MEMS sensors because they can be fabricated using existing techniques. High sensitivity, low power consumption, simplicity in design, low drift and low-temperature dependence are a few advantages capacitive sensing offers relative to other types [16, 22]. Equation 2 shows how the capacitance is related to the geometry of the structure and the dielectric between the plates of

the capacitor.

$$C = \frac{\varepsilon \times A}{d} \tag{2}$$

As seen in the equation, either a change in gap distance, d, change in overlapping area, A, or a change in permittivity, ε, of the dielectric between the plates can cause a change in capacitance, C. Once the capacitance of the MEMS sensor changes the charge is redistributed across the entire circuit and consequentially then be measured by a change in voltage across the capacitor. In a differential capacitance configuration (fig. 5), a small deflection will create two equal in magnitude but opposite changes in capacitance of the two capacitors. When the capacitances change, the charges on the plates are displaced and create equal currents. These currents can be converted into a differential voltage that can be used to sense the displacement of the MEMS [23].

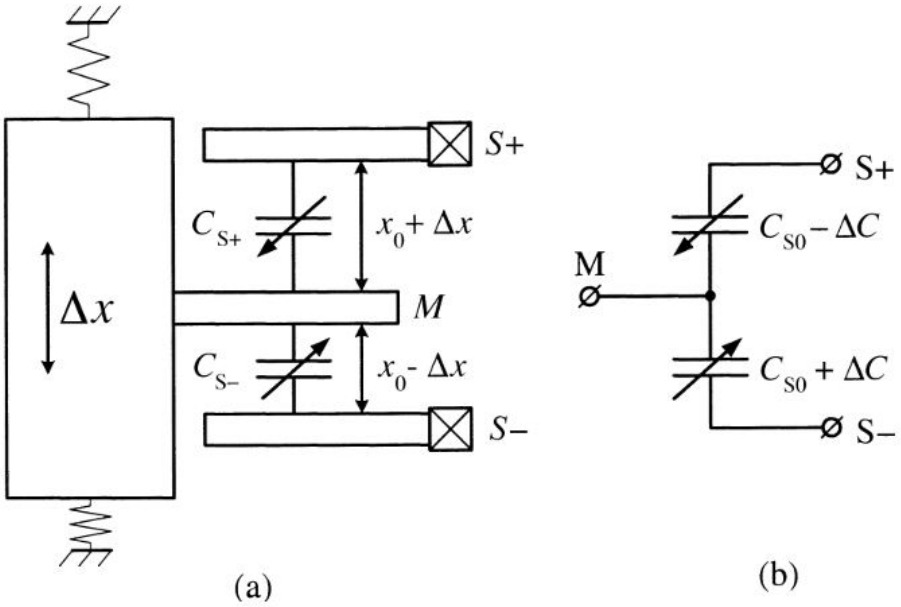


Figure 5: Differential capacitance mechanical configuration (a) and electrical representation (b) [23].

2.3 Electrostatic MEMS Circuits

Interface circuits are important for transducing signals to or from MEMS. For electrostatic MEMS, the signals are transduced from the electrical domain to the mechanical domain in actuators and vice versa in sensors. In order to actuate electrostatic MEMS, a significantly strong electrostatic force is applied across the capacitor structure. This signal is usually a high voltage, low current control signal. The actuation signal can come in the form of a digital signal or an analog signal. Whether a digital or analog control is chosen depends on the application needs.

MEMS that only need to be turned on or off like a switch require simple digital control. A great example of a MEMS switch in practice is the Digital Light Processing (DLP) projector (fig. 6), where the switch controls whether a mirror reflects light out of a projector or not. Most devices on the other hand require a more complex analog control signal. One example of a complex electrostatic MEMS is a deformable mirror (fig. 7) [25]. Generally, these type of devices require a high precision digital-to-

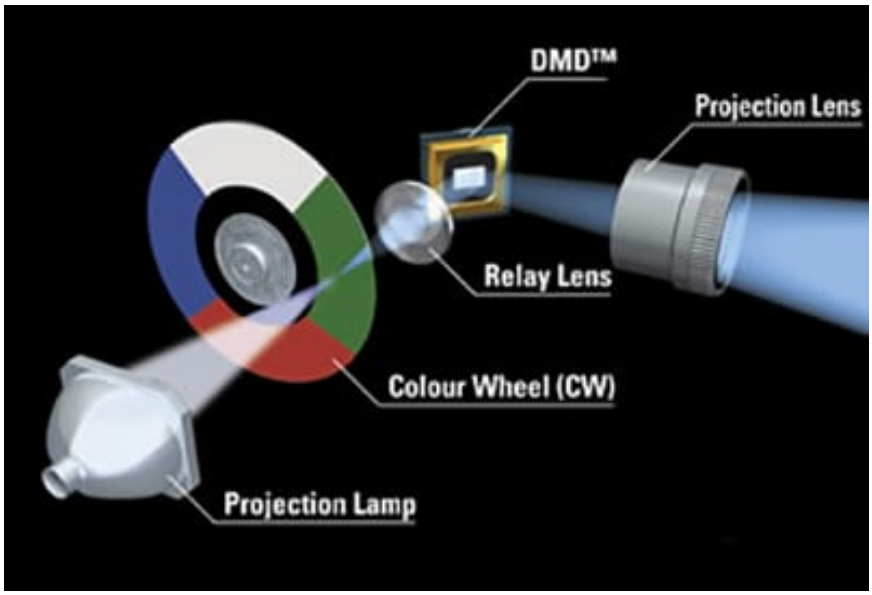


Figure 6: Example of the operation of a DLP® Projector using digital micro-mirror devices (DMD) [24].

analog converter (DAC), a linear, high voltage (HV) amplifier, and complex interface circuitry [26].

On the other hand, electrostatic devices that are used as sensors require different circuits. Although the goal in this case is to measure instead of actuate, a reference signal is still used and sensing is performed. In many cases the sensing signal is a small ac signal superimposed on a bias dc voltage, the exception is force feedback design which measures the amount of force needed to keep the device in its "zero" position. The front end circuit interface is very important because its task is to read the mechanical change of the sensor as an electrical change in the circuit. A common front end circuit used for estimating capacitance is the charge-to-voltage converter [23, 28]. In this case, when the device capacitance changes due to a stimulus, the change is detected by integration of the actuator current. This is possible because the change in capacitance causes a redistribution of charge that is detected by the charge-to-voltage converter. This circuit can be used in a single sided or differential design. One of the challenges of this interface circuit is the lack of sensitivity due to the small magnitude and drift of the output voltage associated with charge-to-voltage converters [29, 30]. Other capacitive sensor interface circuits include the following: wheatstone bridge, DC bias sensing, diode-quad sensing, opposite excitation sensing,

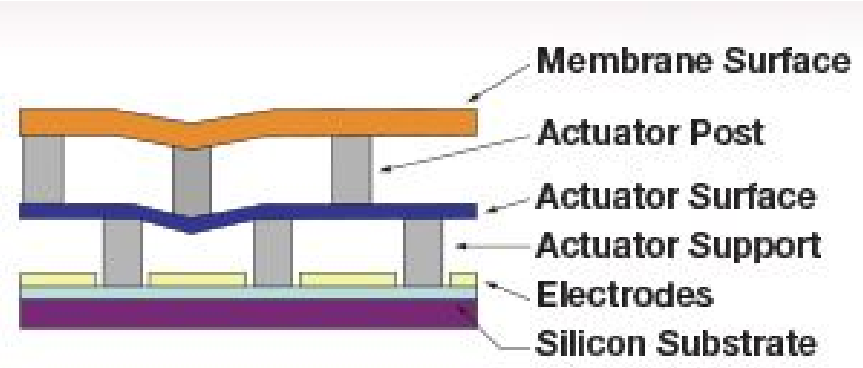


Figure 7: Example of a deformable mirror [27].

forced-balanced sensing, switched capacitor sensing, frequency sensing, sigma delta modulation, correlated double sampling, and chopper stabilized [31, 23].

Furthermore, research is being done in order to enable simultaneous actuation and sensing, which is accomplished by extracting features from the electrical response of the electrostatic actuator to a reference signal. One example of research in this area is capacitive charge-based self-sensing for resonant electrostatic MEMS mirrors [32]. In this case, simultaneous actuation and sensing uses a square wave to change the angle of the device while a charge to voltage integrator measures the redistribution of charge. This is one example of many other methods in this area [33, 34, 35, 36]. Simultaneous actuation and sensing is an important research area as it allows for feedback control of MEMS.

Feedback control of MEMS require a robust actuation and sensing system. A simultaneous actuation and sensing system that uses a DC drive signal and an AC sense signal is commonly used. For this thesis, the system uses a PWM signal as both the drive signal to actuate the MEMS and the sense signal to estimate the capacitance or displacement. The sense signal is measured using a capacitor divider interface circuit, which is one of several methods for obtaining a sense signal. The capacitor divider was chosen over other interface circuits because of its simplicity and compatibility with PWM signals. When a PWM signal passes through a capacitor divider, a PWM signal with a smaller amplitude is produced. The only characteristic of the PWM signal that needs to be tracked is the amplitude. Before further investigation, it is important to understand the background research previously accomplished regarding both the PWM signal and the capacitor divider as the interface circuit for electrostatic MEMS.

The capacitor divider as a sensing circuit was first researched in 2008 by the Universitat Politecnica de Catalunya team led by Daniel Fernandez [30]. A capacitor

divider circuit is simply two capacitors in series where the output voltage is measured between the capacitors. This application is exactly the same as a resistor divider circuit except in this case the impedance is in the form of capacitors (fig. 8). The drive signal is a pulsed signal. Given the input voltage, V_A, output voltage V_B, and the reference capacitor value, C_s, the unknown changing capacitance, C(t), can be estimated using the following equation.

$$C(t) = \frac{V_A - V_B}{V_B} \times C_s \tag{3}$$

If C(t) and C_s, as shown in eq. (4), were swapped, the equation would be the following.

$$C(t) = \frac{V_B}{V_A - V_B} \times C_s \tag{4}$$

In these equations it is assumed that the parasitic capacitance, C_p, is negligible and the initial voltage at V_B is zero. According to their work, there are two important conditions that are necessary to make this sensing circuit function properly. The first condition is that the known/reference capacitance has to be significantly larger than the estimated capacitance of the MEMS. This is important because when the voltage

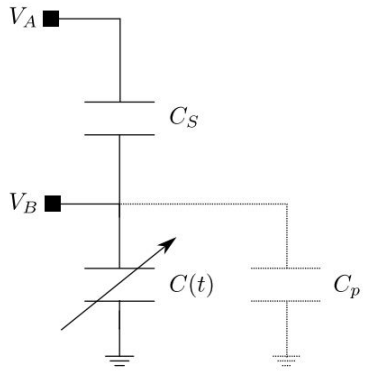


Figure 8: The capacitor divider circuit with a parasitic capacitance [37].

is divided across the capacitor divider circuit, more voltage is distributed across the smaller capacitor and a smaller amount of voltage is distributed across the larger capacitor. This allows for a large applied voltage across the MEMS and thus a large enough force for actuation. If the voltage across the electrostatic MEMS is too small then no or minimal actuation will occur [30]. The second condition for the capacitor divider circuit is that the drive signal can not have too high of a frequency otherwise the capacitors will not be able to charge and discharge fast enough to divide the input signal. The capacitance divider circuit complements the PWM signal as a single signal can be used to actuate and estimate the capacitance of the device. The capacitance divider and an electrostatic actuator were both simulated in Spectre®, a Cadence® SPICE and component model simulation software, and experimentally tested. The first simulation performed was a transient simulation of the distance between the plates an electrostatic actuator and the circuit output voltage. The simulation results proved that the interface circuit gave output voltages that corresponded with the change in capacitance (which can be derived from the distance between the two plates) of the electrostatic actuator. Fernandez then demonstrated in a simulation that the capacitor divider circuit could be used in a pulsed digital oscillator feedback architecture. In the experimental tests, Fernandez built the circuit on a 3.3 V, 0.35 μm CMOS 2P5M technology and tested it on fixed capacitors [30]. The system parameters were a voltage input of 3 V, a duty cycle of 99%, frequency of 100 kHz, and reference capacitance at 100 pF. The variable capacitors used were fixed capacitors at 1, 2, 3, 4 and 5 pF. The experimental results showed that good linearity was obtained between the output voltages and the change in capacitance of the devices. However, this interface circuit suffers from leakages associated with the transistors used in their system.

In 2019, a team, led by Corey Pollock, experimentally verified how using a PWM

signal can be used to achieve analog control over electrostatic MEMS [26]. In order for a PWM signal to be usable there is one constraint that the signal needs to meet. This constraint is that the operating PWM frequency has a limited bandwidth. The lowerbound frequency is limited by the mechanical resonant frequency of the MEMS. If the frequency is set below or at the mechanical resonant frequency then the position of the MEMS will not have a steady state position but instead is constantly moving with the signal. By having the frequency above the mechanical resonant frequency, the MEMS will maintain a steady state position that varies only with the duty cycle. On the other hand the upperbound frequency limit is restricted by the electronic response time of the capacitive actuators. Intuitively, one can reason that this limit exists because if the signal switches too fast for the capacitive actuators to charge then there will be no electrical force to actuate. After delineating the requirements of the drive signal, Pollock goes on to test the PWM drive signal on electrostatic MEMS. Pollock tested the PWM drive signal on three devices; a parallel plate, a comb drive, and a commercial deformable mirror. In summary, the PWM drive was able to achieve comparative performance (in terms of actuation range) as the conventional analog open loop control. Another discovery was that, depending on both the device and applied voltage amplitude, the positional response can be linearly controlled by the duty cycle. Lastly, the PWM control circuit is smaller and more economical than conventional analog control circuits. A traditional analog circuit requires a high precision DAC and a linear HV amplifier, which can be quite expensive. A PWM drive signal does not require these two parts because the signal can be generated by controlling when the timing switches are on and off [26]. By combining the PWM drive signal and capacitance divider circuit, a feedback control system for MEMS is possible.

III. Methodology

3.1 Preamble

In this section, the methodology used to investigate the PWM driven simultaneous actuation and sensing system will be described.

3.2 System Overview

In general, the simultaneous actuation and sensing system is divided into four main components (fig. 9): driving circuit, electrostatic MEMS, sensing interface, and signal processing circuit. The driving circuit block is responsible for the drive signal that actuates the electrostatic MEMS and also serves as the modulation signal that the sensing block will use. For this thesis, the intention was to use basic electrostatic MEMS types, like parallel plate capacitors and electrostatic combs. The sensing interface block is in charge of extracting useable signal characteristics that can be used to infer the position of the actuated device. Lastly, the signal processing block is responsible for refining the signals coming from the sensing interface in order to make them easier to use. For this thesis, there are two requirements: a PWM drive signal and a capacitor divider circuit. In this model, the core components are the drive signal circuit, MEMS, and the sensing interface because these three components are the only things necessary to simultaneously actuate and sense a MEMS when its position changes. Whereas the signal processing block is superfluous as it refines the

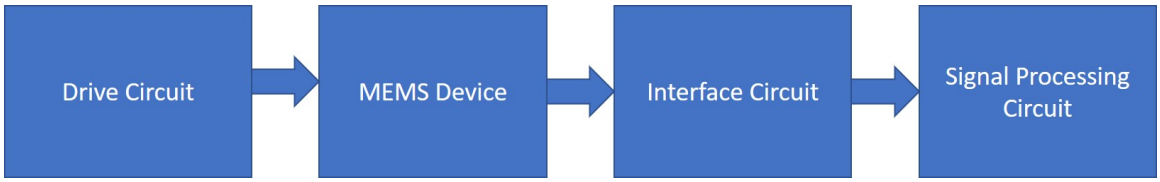


Figure 9: System overview of electrostatic drive and sense system.

output signals from the interface circuit into a signal that provides more accurate and precise measurements. The main focus of the methodology section will be describing the process used to design and test the system.

3.3 Integration of Electrostatic MEMS Devices

The research used parallel plate electrostatic actuators. Parallel plate actuators were mainly used because they are one of the most simple actuators. The equations used to describe the electrostatic force and the mechanical dynamics are therefore simple. Moreover, the displacement is in the out-of-plane direction which can be measured using a ZYGO® white light interferometer machine. A white light interferometer is a machine that uses an incidental and reflected light beam on a target to recreate a 3D surface profile. The ZYGO® interferometer used in this project was the ZYGO® NewView 7300 as seen in Figure 10.

The devices were not custom made for this project and instead were taken from AFIT's inventory of extra chips. From the inventory, two chips were chosen which had suitable parallel plate actuators on them. When MEMS chips are stored, they are sent with a film of photoresist to prevent damage to the devices. When a chip is ready to be used, the photoresist film needs to first be removed by acetone. Next, a release process is done to remove the sacrificial oxidation layer and free the MEMS for actuation. The release process used for the devices was the wet release, which has two steps. After removing the protective photoresist film using acetone, the chips are placed into 49 percent HF solution for eight minutes where the Si02 is etched away. Next, the chips are placed into a methanol beaker where the residual mixture if HF, SiO2, and DI water is rinsed off. It is important that after using HF, the chips are always maintained submerged in methanol until placed into the CO2 dryer methanol filled chamber. The CO2 dryer is important because it is used to dry the

Figure 10: Zygo NewView 7300.

chips without causing stiction through the critical point drying technique. Stiction (more specifically release-related stiction) takes place when you remove a sacrificial later during fabrication and is usually caused by capillary force. This phenomenon prevents the mobile plate from actuating. One important thing to note is that the MEMS are wirebonded to a dual line package in order to make it easier to perform testing using protoboards. The Hybond model 626 (fig. 11) was used to wirebond the devices using gold lines.

When trying to accomplish this task there were many challenges that led to the inability of using MEMS in the circuit. The first challenge occured during the wirebonding process. Since the devices on the chip were not specifically designed for wirebonding, the bonding pads were too small and too close to the devices. This would cause the bonds to not adhere. Each failed adhesion caused the pads to be less usable. Also, since the pads were so close to the device each attempt to bond

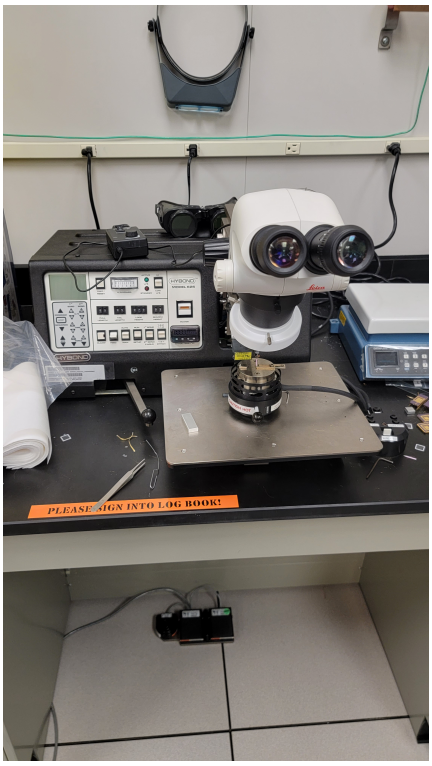


Figure 11: Hybond model 626 wirebonder.

had a high chance of breaking a leg of the device. This destroyed many devices. Another roadblock was that the chips that I created suffered from stiction due to not being released properly and they were also poorly designed. The poor design was that the fixed plate was divided into two separate plates. This was a mistake because it doubled the risk of failure because I had to wirebond the device for both fixed plates instead of just one. Another issue that occurred was that when actuating the devices, the poly-silicon layers would fuse together following a pull-in. Unfortunately, for these reasons all the chips became unusable. From this experience, I would do a couple things differently. First, I would move the bonding pads farther from the devices to prevent damage during wirebonding. Second, I would use the substrate layer as the fixed plate because the silicon nitride layer on top of the substrate will prevent stiction from occurring during pull-in. As a result, instead of using a MEMS, regular capacitors and trimmer capacitors were used as stand-ins. Since the focus of this

research is to design and evaluate a system that can detect a change in capacitance, a MEMS is not required.

3.4 Variables of interest

Next, the variables of interest were identified. Figure 12 shows an overview of the input factors and output metrics of the system.

Input factors were chosen based on a best guess on what factors could influence the output signals. The factors can be divided into two categories: drive factors and sense factors. The drive factors are derived from controllable factors in the PWM drive portion of the system as shown in Figure 13. Likewise the sense factor is derived from the sensing interface. Something to note is that the drive signal factors are dependent on the signal characteristics and not physical characteristics, whereas the sensing factors are based on a ratio of the physical components and signal processing.

3.4.1 Input Factors

Input Factor Descriptions:

- PWM frequency (Drive Factor): This factor influences the speed of response. Prior research, shows that the frequency range is bounded by the resonant frequency on the lower limit and electronic response time on the upper limit. Increasing the frequency reduces the effect leakage has on the output of the

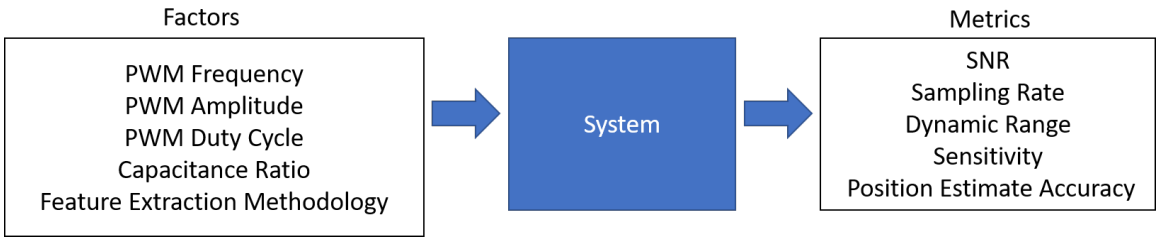


Figure 12: Factors and metrics of proposed system.

signals [37].

- PWM amplitude (Drive Factor): This factor influences the actuation distance, resolution, power, and electrostatic force.
- PWM pulse width/duty cycle (Drive Factor): This factor influences the amount of time that voltage is applied to the MEMS which alters its displacement.
- Device capacitance to reference capacitor (Cs/Cref) ratio (Sensing Factor): This factor affects the amount of voltage applied to the MEMS and the resolution of the change detected.
- Feature extraction/processing method (Sensing Factor): This factor influences how the signal is handled after the interface circuit and what the final output will look like.

There are two configurations of the capacitance divider interface. As shown in figure 14, Cs can be placed either in the top or the bottom of the series connection, creating 2 different cases. This is important because the capacitance ratio produces a different effect on the output signal in each case. As seen in figure 15(a), when the capacitance ratio becomes smaller, the output voltage tends towards zero. On

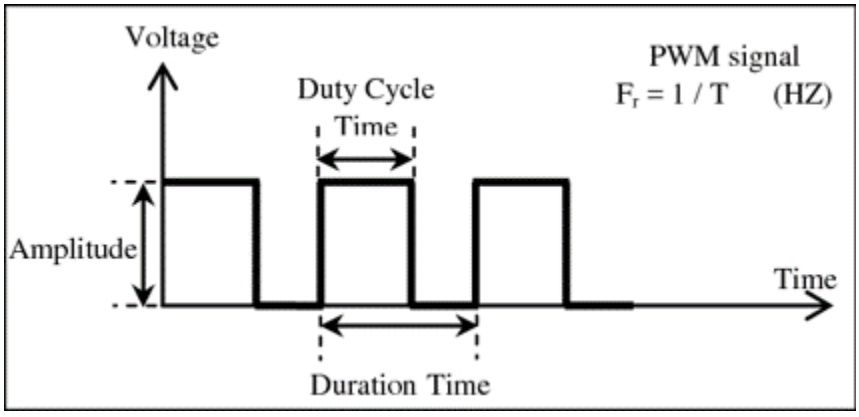


Figure 13: PWM Signal Characteristics [38].

the other hand, when the capacitance ratio is high, the output voltage tends towards the maximum voltage which is limited by the input amplitude (fig. 15(b)). This is important because it shows what kind of signal is expected at the output based on each case. At smaller capacitance ratios, in case 1, the output will have a very low amplitude, whereas in case 2 the output will have a very high amplitude. Another important note of interest is that in both cases at low capacitance ratio, a larger portion of the input voltage is applied to sense capacitor. In case 1, Vin-Vout is the applied voltage across Cs. Whereas in case 2, Vout is the voltage across Cs. This is important because it shows that in both cases having a low capacitance ratio allows

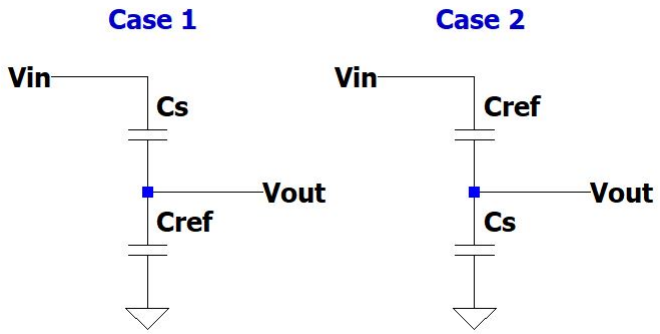
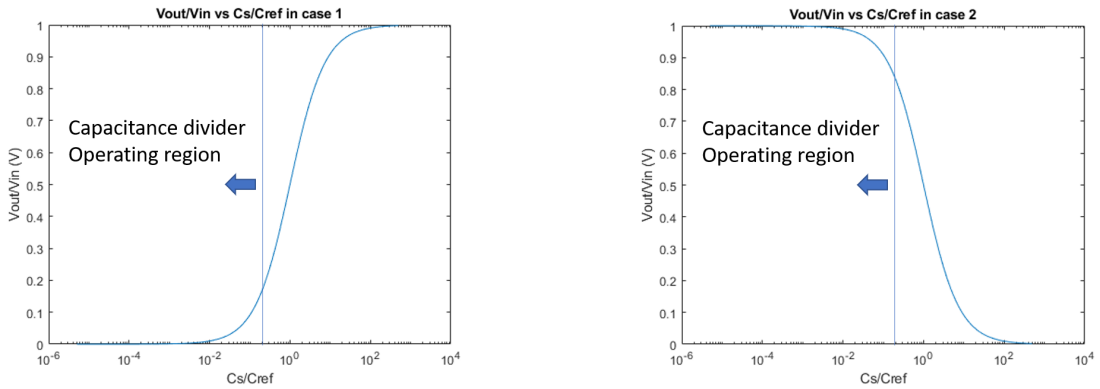


Figure 14: Capacitor Dividor Sensor placements variations. Cs represents the Electrostatic MEMS capacitor and Cref represents the reference capacitor.



(a) Vout in Case 1

(b) Vout in Case 2

Figure 15: Vout vs Cs/Cref for both capacitor divider variants. 1:10 ratio was used as the upperbound cutoff because this was the ratio used in previous research [37].

for an efficient transfer of voltage to be applied to the the device. On the other hand, a higher ratio would require a much larger input voltage amplitude to apply the same amount of voltage across the device. Although reducing the capacitance ratio to as small as possible is important, this also effects the resolution. In reality, at any point on the curve Vout detected at each ratio will be a little bit above and below the ideal curve due to noise and other non-idealities. Therefore, as the capacitance ratio deviates from unity, the slope of the change in capacitance becomes smaller and less perceptible. As a result, it is important to choose a capacitance ratio that is not too small that the change in capacitance of the MEMS cannot be detected. Therefore, there is a tradeoff between the resolution and actuation voltage across the capacitor.

3.4.2 Response Variables

As seen in figure 12, the following response variables are used to measure the performance tradespace of the system. The response variables chosen as the metrics are as follows: signal-to-noise ratio (SNR), sensitivity, sampling rate, change in capacitance estimate accuracy, and dynamic range. The SNR is the average signal power divided by average noise power. The sampling rate is the number of samples taken per second and determines how fast the system responds. Sensitivity is the measure of the change in output based on the change in input. Capacitance estimate accuracy measures how close the obtained estimate of the capacitance is from the true capacitance. Lastly, the dynamic range is the controllable range of the system input factors.

3.5 Simulation and Test

3.5.1 Preliminary Verification

The first step is to build a model using ideal components as seen in Figure 16. In its most basic form, the proposed control circuit is made up of an ideal PWM signal source and two ideal capacitors in series. The ideal PWM has no noise and zero rise time. The ideal capacitors are pure capacitors with no leakage, resistances, or inductances. LTspice® was used to simulate the circuit. This was done in order to make sure that LTspice works.

This step is done in order to ensure that an unknown capacitance will be able to be extracted from the signal. In this stage the reference capacitor was placed on the bottom of the capacitor divider circuit because it would force the output voltage to be a much smaller. This decision was made in order to have as much of the input voltage applied across the device. The next step taken was to do a small test to see if the capacitor divider circuit could be used to detect a change in capacitance.

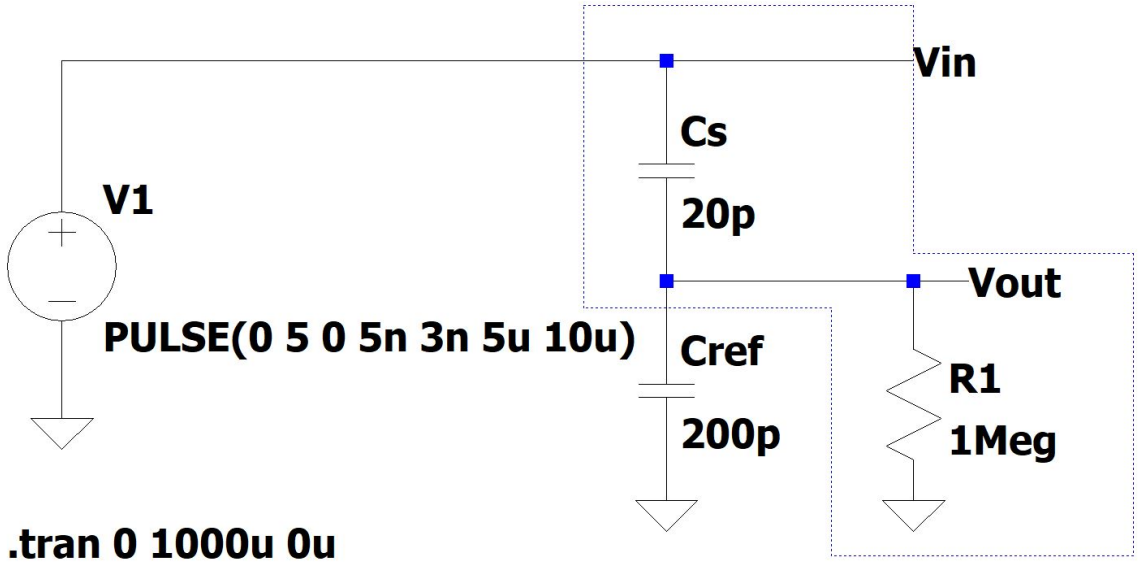


Figure 16: LTspice® model of the basic circuit with ideal components

In order to verify if the basic circuit can detect a change in capacitance, a quick experimental test was performed by using a trimmer capacitor, as the varying capacitance, in series with a capacitor and hooked up to the waveform generator as seen in fig. 17. A two factor analysis of variance ANOVA test was conducted on this data in order to test which factors may produce a statistically response in the output. The two factors varied were the trimmer position and the duty cycle of the signal. Where the trimmer position had four different treatments and the duty cycle had three different treatments, 25%, 50%, and 75% as seen in Table 1. This produced 12 different combinations. The test was done with four replications and the capacitance estimation data obtained from the experiments was analyzed using R statistical software.

The next step after the ideal basic circuit was to build the circuit using real parts, one subsection at a time, until the full circuit was created.

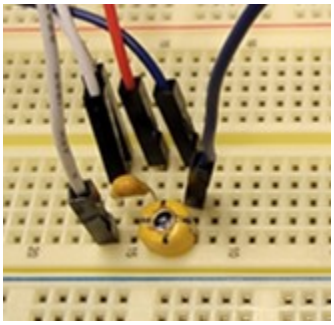


Figure 17: Experimental capacitor divider circuit with trimmer capacitor.

Table 1: Anova Factors and Treatment Level Combinations

		Trimmer Position			
		Position 1	Position 2	Position 3	Position 4
Duty Cycle	25%	1	2	3	4
	50%	5	6	7	8
	75%	9	10	11	12

3.5.2 Drive Circuit Block

The first section incorporated was the the drive circuit. The drive circuit is the same circuit used by Pollock [26]. The circuit contains a high voltage MOSFET driver that transforms a small voltage PWM signal into a high voltage PWM signal. The reason a waveform generator is not usable as a stand alone PWM source is because many MEMS require high voltages that the waveform generator cannot supply (maximum amplitude of 5 volts). A HV amplifier is not used for two reasons. The available HV amplifiers had very low bandwidths and therefore could not respond quickly enough for a PWM signal. The second reason is that HV amplifiers are way more expensive than a MOSFET driver circuit. By incorporating real components to the model, nonidealities are introduced into the system. Some nonidealities are finite rise times, finite response delays, noise, and frequency dependent impedances. The first section of the nonideal drive circuit is the PWM voltage source. The waveform generator has an 80 MHz frequency limit. The ideal voltage source has unlimited bandwidth. In order to make a realistic PWM signal, a Laplace transform needs to be done on the signal to reduce the frequencies used in creating the PWM signal. Another nonideality included is the 50 ohm series resistance and transmission line. Next, the MOSFET driver circuit was added. For this portion the LTC4444 sample circuit found in the LTspice® model library was used as the base to design the MOSFET driver circuit (fig. 18).

After creating the model of the drive circuit, the next step is to test the circuit with real drive components. The initial test for this was done using individual circuit board components in order to better understand the generated drive waveform. In subsequent tests a printed circuit board (PCB) was fabricated in order to increase the reliability of the generated signal. The PCB was designed using Kicad® and manufactured by an external vendor. After the boards were received, the circuit

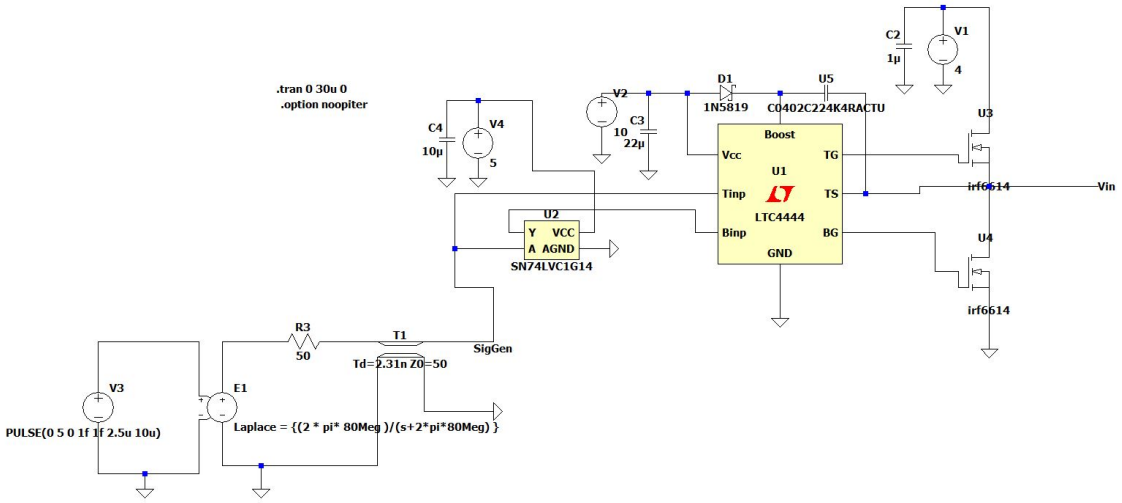


Figure 18: LTspice® model of the PWM Drive Circuit.

components and connectors were soldered onto the board to create the final PCB (fig. 19).

The oscilloscope, LECROY® Wavemaster804zi, was used to measure the output

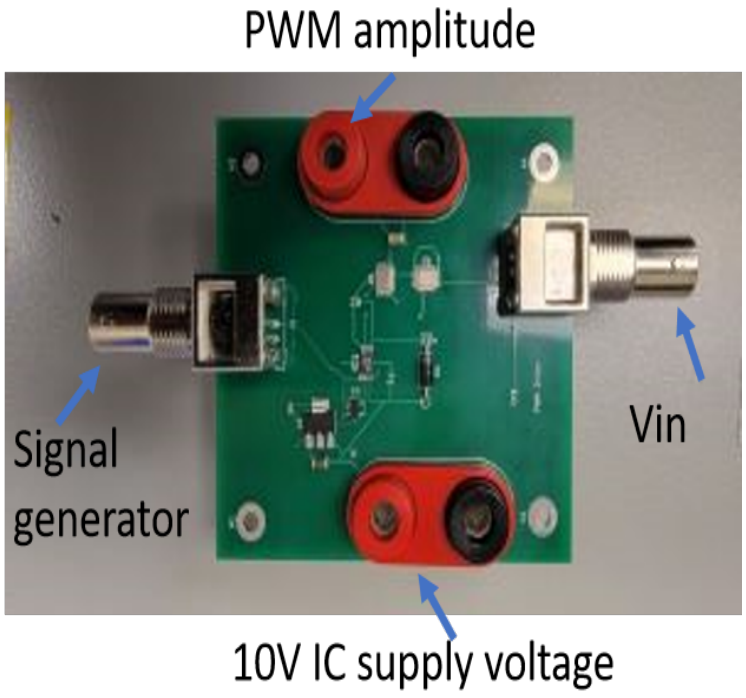


Figure 19: Picture of a completed PCB that contains the MOSFET Driver circuit.

signals from the experimental circuits. As can be seen in the figure, there are two DC voltage sources and one waveform generator that are hooked up to the MOSFET PCB. The Agilent® E3631A Triple Output DC Power supply is used to power the integrated circuit (IC) chips and is set to 10 V. The Agilent® U3606A is used to set the PWM amplitude and can be anywhere from 0 V to approximately 30 V (60 V is the true maximum amplitude which is due to the series MOSFETs which have 60 V ratings each). The output is connected by a junction connector that can be connected directly to the oscilloscope during operation. Figure 20 shows the complete test setup.

After completing the experimental test setup, the output of the experimental MOSFET driver circuit was saved and compared to the simulation data. This was done to verify that the simulation is an accurate representation of the real circuit. Through comparisons, differences were identified and resolved.

Once confidence in the model was obtained, the next step was to incorporate the interface circuit with the trimmer capacitors to emulate the MEMS to the drive

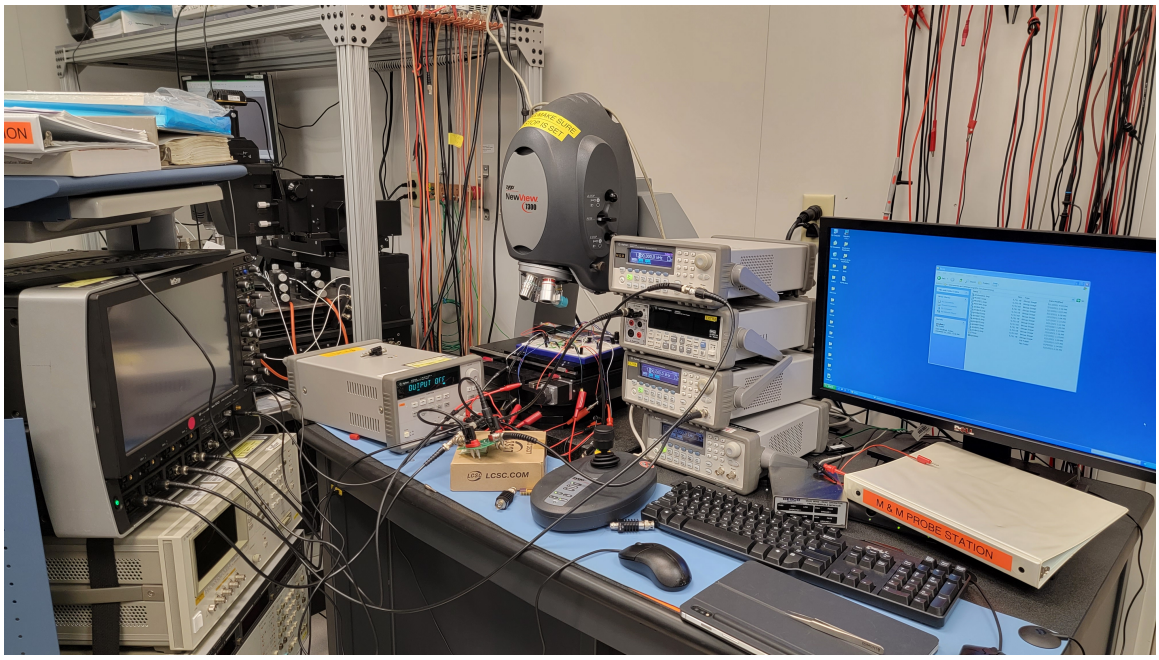


Figure 20: Total experimental Setup.

circuit. This was relatively simple because the capacitor divider circuit is simply two capacitors in series. Figure 21 shows the complete LTspice® model of the circuit. With these subsystems combined, the essential parts of the simultaneous actuation and sensing system were integrated. At this stage, it was important to analyze the signal outputs and glean information on the characteristics that dominate how the system functions. This information guided the decision making for the subsequent signal processing steps.

3.5.3 Signal Processing Block

After verifying the main circuit performs as intended, the next step was to plan out the signal processing block of the system. As can be seen in figure 22, the output voltages from the interface circuit are sent into an analog processing circuit. The role of the analog processing circuit is to process the voltage signals into consistent and clean signals for the ADC by filtering out noise and ringing and then scaling the signals into the ADC input range. Once the ADC converts the analog signals into digital signals, the capacitance estimate can then computed through the digital signal

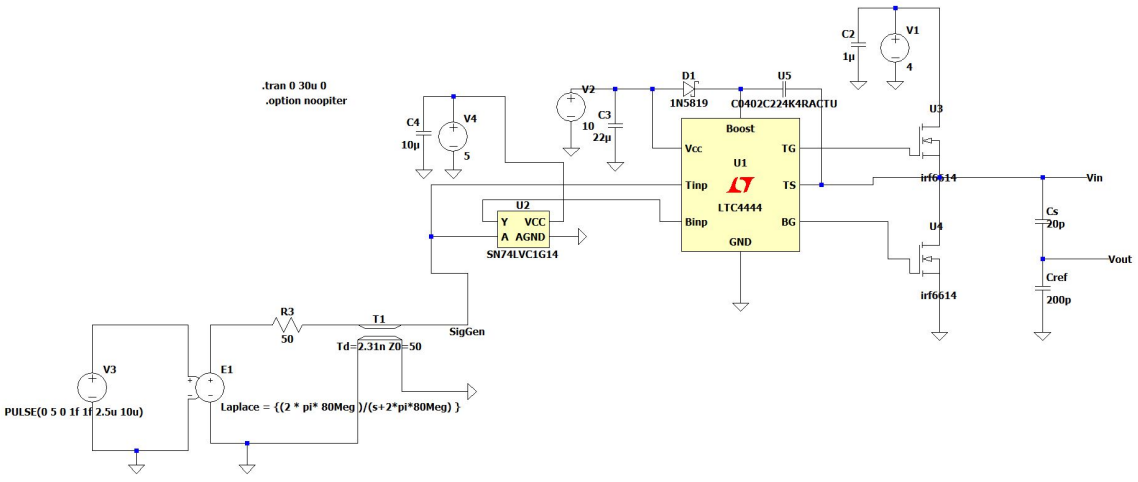


Figure 21: LTspice® model of the PWM drive and capacitor divider circuit.

processing block. As the ADC and digital signal processing block roles can be done by a microcontroller, the primary focus of this section is designing the analog signal processing block for the two variants of the capacitor divider circuit shown in Figure 23.

3.5.3.1 All Pass Filter Analog Circuit Design

This section focuses on the design of the all pass filter variant of the capacitor divider interface circuit which requires a high impedance measurement circuit. One design choice made was to have the capacitor divider circuit be configured with the sense capacitor in the top position of the interface circuit, as seen in case 1 in Figure 14. This configuration produces a low voltage signal which is more beneficial than the high voltage signal produced in case 2. This is because the high impedance buffer opamp circuit cannot handle voltage signals that are higher than the rail voltages which would occur in case 2. In order to limit the sampling rate of an ADC, which

Figure 22: Signal Processing Flow Chart.

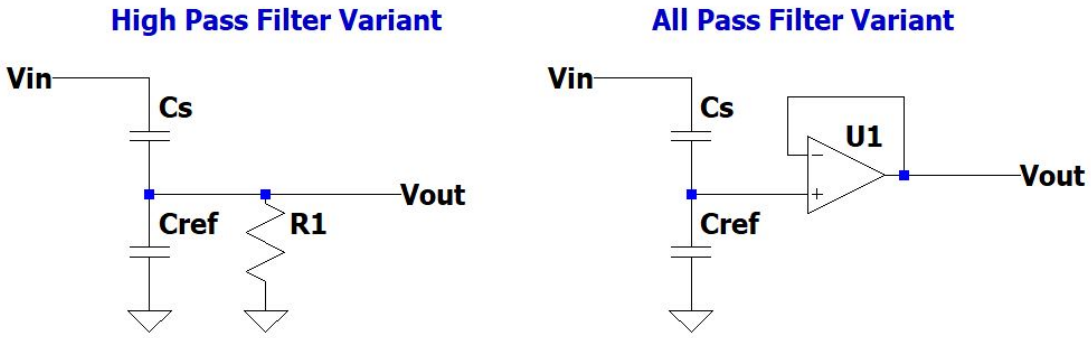
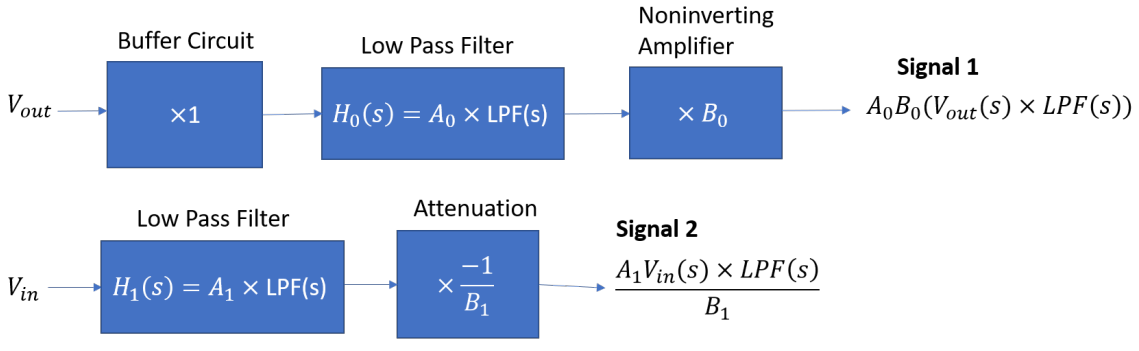


Figure 23: High Pass Filter Variant and All Pass Filter variant of the capacitor divider.

will be incorporated in the future, only one sample at most on each channel was used per drive cycle in measuring the capacitance. The last design choice was to have two output signals that can be used to estimate the capacitance using the capacitor divider equation (eq. (4)).

The first step in designing the analog signal processing circuit is to plan out each step that would be needed to accomplish the above requirements. This can be accomplished by creating a block flowchart as seen in Figures 24 and 25. As a reminder, the two output signals from the capacitor divider circuit are V_{out} and V_{in}. V_{out} is the signal produced by the capacitor divider and V_{in} is the PWM drive signal that is sent into the capacitor divider. The two signal paths that stem from them will be referred to as Signal 1 and Signal 2, respectively. Together, the signals are used to estimate the capacitance. This thesis explores two different circuits to process the signal: PWM amplitude scaling (fig. 24) and amplitude integrating (fig. 25).

First, the all pass filter amplitude flowchart (fig. 24) is explained. In Signal 1's path, V_{out} is fed into a buffer circuit. This is to mitigate a low pass filter circuit that blocks the DC bias found in PWM signals. This fulfills the first requirement of



$$C_{estimate} = \frac{V(Signal\ 1) \times \frac{1}{A_0B_0}}{V(Signal\ 2) \times \frac{B_1}{A_1} - V(Signal\ 1) \times \frac{1}{A_0B_0}} \times C_{ref}$$

Figure 24: Amplitude scaling flowchart.

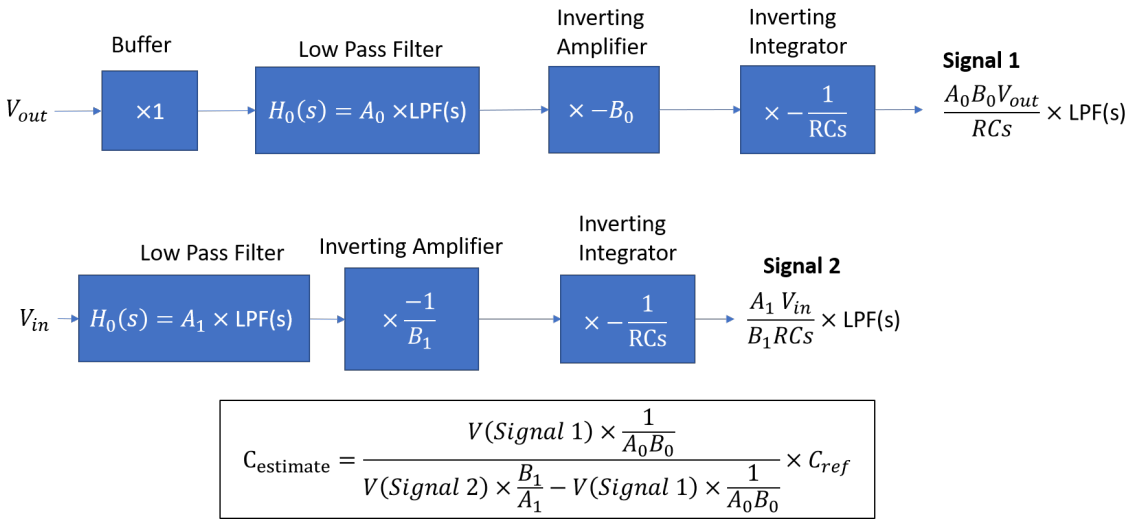


Figure 25: Amplitude integrating flowchart.

creating a high impedance measurement circuit. Next, Signal 1 passes through the low pass filter. The low pass filter's job is to smooth out the signal by removing high frequency noise and ringing. Signal 1 is scaled by the filter gain factor, A_0. The point of amplification is to make full use of the input range of the ADC (0V to 3.3V or 5V which are the typical ranges of an ADC). For a variable capacitor, this is accomplished by making sure the largest possible capacitance correlates with the largest ADC input voltage. In Signal 2's path, Vin is fed to the low pass filter to smooth out noise and ringing from the signal. Then the signal is attenuated to fit into the input voltage range of the ADC. From both Signal 1 and Signal 2, the output signals should still be PWM signals but with different amplitudes. The ADC should sample the output voltages only once at most during the on cycle of the output signal.

Next, the all pass filter integrating flowchart (fig. 25) is explained. Signal 1 and Signal 2 paths are made of the same building blocks: a low pass filter, an inverting amplifier, and an inverting integrator. Except, Signal 1 starts with a buffer. The combination of the inverting amplifier and inverting integrator serves two purposes. The first purpose is to have a positive output signal. Second, in the case for Signal

1 where the signal is a low voltage signal, the amplifier will increase the rate of charge of the integrator. This will allow flexibility when designing the circuit because the inverting amplifier and the inverting integrator components can be altered either individually or as a combination in order to produce the required output signal. The final signals will be of the form of an angled step for each period of integration. One important aspect of an integrator is the need to have a reset signal in order to discharge the integrator capacitor before the opamp saturates. The integrator circuit can be reset after one period of the PWM cycle or after multiple periods. The integrators have to be sampled before the integrators are reset. The reset signal used was a drive period long off signal. It is important to look at the influence of sampling after one PWM period or multiple periods.

Finally, both flowcharts provide two signals that can be used to estimate the capacitance of the capacitor. For both flowcharts, we can use the following equations to estimate the capacitance by using the output voltages received from both Signal 1 and 2, V(Signal1) and V(Signal2), respectively. This is possible because the transformations in the flowcharts permit us to indirectly determine V_{out} and V_{in}.

$$V_{\text{out}} = \frac{V(Signal1)}{A_0 \times B_0} \tag{5}$$

$$V_{\text{in}} = \frac{V(Signal2)}{A_1/B_1} \tag{6}$$

$$Cs = \frac{V_{\text{out}}}{V_{\text{in}} - V_{\text{out}}} \times Cref \tag{7}$$

In equation 5, V_{out} can be estimated by dividing the V(Signal1) by the low pass filter gain, A_0, and noninverting amplifier gain, B_0. Similarly, in eq. (6), V_{in} can be estimated by dividing the V(Signal2) by the low pass filter gain, A_1, and multiply

by the attenuation gain, B_1. Next the estimated, V_{out} and V_{in} values can be used with the reference capacitor, Cref, in equation 7 to estimate the sense capacitor, Cs. These calculations may be efficiently and quickly done through the digital processing circuit of a microcontroller. After designing the signal blocks, the next step is to design the circuit that will realize the signal processing block. Figure 26 shows the circuit design for the all pass filter amplitude scaling circuit and, Figure 27 shows the all pass filter integrator circuit. The gain values of both circuits are shown in Table 2. One important thing to point out is that the all pass filter variant requires a switch that is connected to ground on the V_{out} node. This switch should turn on during the off cycle of the PWM signal. This prevents the node from drifting from zero volts during an off cycle.

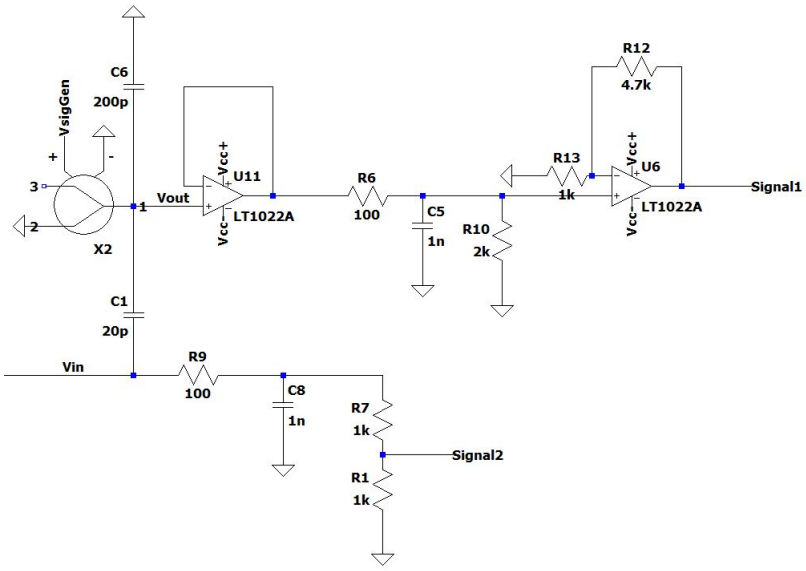


Figure 26: All pass filter amplitude scaling circuit

Table 2: All Pass Filter Amplitude Gain Values

Circuit	$\mathbf{A_0}$	$\mathbf{B_0}$	$\mathbf{A_1}$	$\mathbf{B_1}$
Scaling	0.952	5.7	0.952	2
Integrating	0.5	10	0.99	0.37

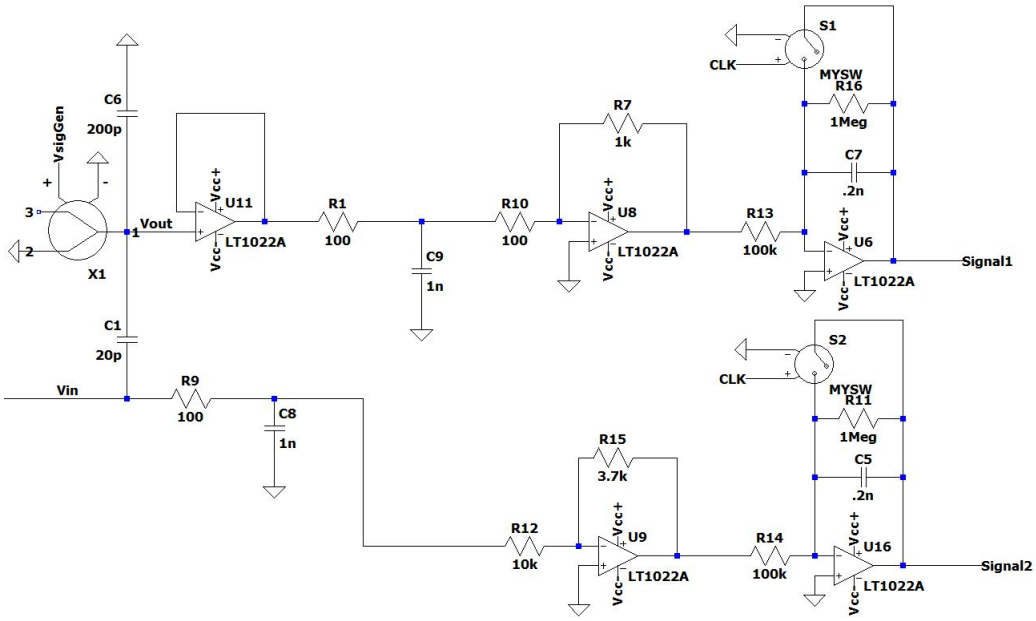


Figure 27: All pass filter amplitude integrating circuit

When combining the signal processing circuit, the complete circuit models for the amplitude scaling circuit and the amplitude integrating circuit are obtained and the complete circuit can be found in Figures 62 and 63 in Appendix A. This can then be used to run a complete simulation of the whole system. All the signal processing circuits were built on a breadboard as seen in Figure 28. After verifying the signal processing circuit simulation produces the intended output signals and is able to estimate the capacitance of the MEMS, the next step is to experimentally test the complete circuit. For this system, testing will be done where the varying factors will only be the capacitance ratio and duty cycle. In order to verify if the circuit works as expected, the capacitance of the device will be compared with the capacitance of the system.

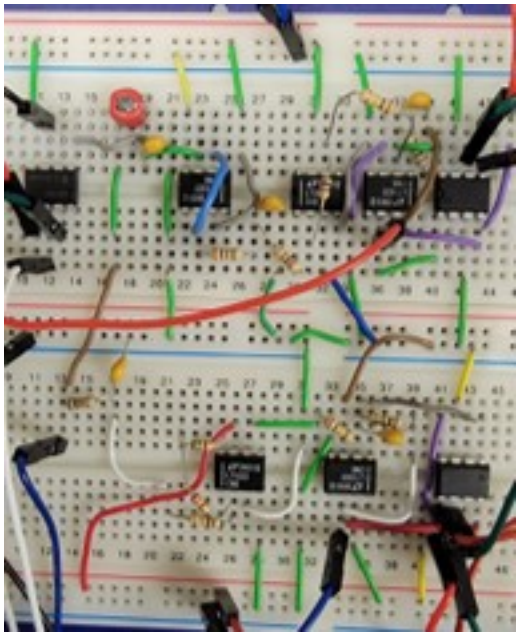


Figure 28: Photo of the experimental amplitude scaling circuit wired on a bread board.

3.5.3.2 High Pass Filter Analog Circuit Design

In this section, the analog circuit design to process the high pass filter variant of the capacitor divider circuit is developed. Like in the previous section, this section starts with flowcharts of an amplitude circuit, Figure 29, and an integrator circuit, Figure 30.

First, the high pass filter amplitude scaling flowchart (fig. 29) is explained. Since the output of the high pass filter variant, V_{out}, is a product of the high pass filter circuit, V_{in} needs to be modified by a similar high pass filter. This is to ensure that Signal 1 and Signal 2 have matching corner frequencies, discharge times, shape, and most importantly the DC portion of the PWM signal are blocked in both signals. We can equate both high pass filters to each other because the PWM signal's frequency composition (without its dc component) is entirely in the high pass band of both filters. As a results, V_{out} is the V_{in} (without its dc component) signal scaled by the capacitance ratio and V_{in2} is simply the V_{in} signal (without its dc component). Next,

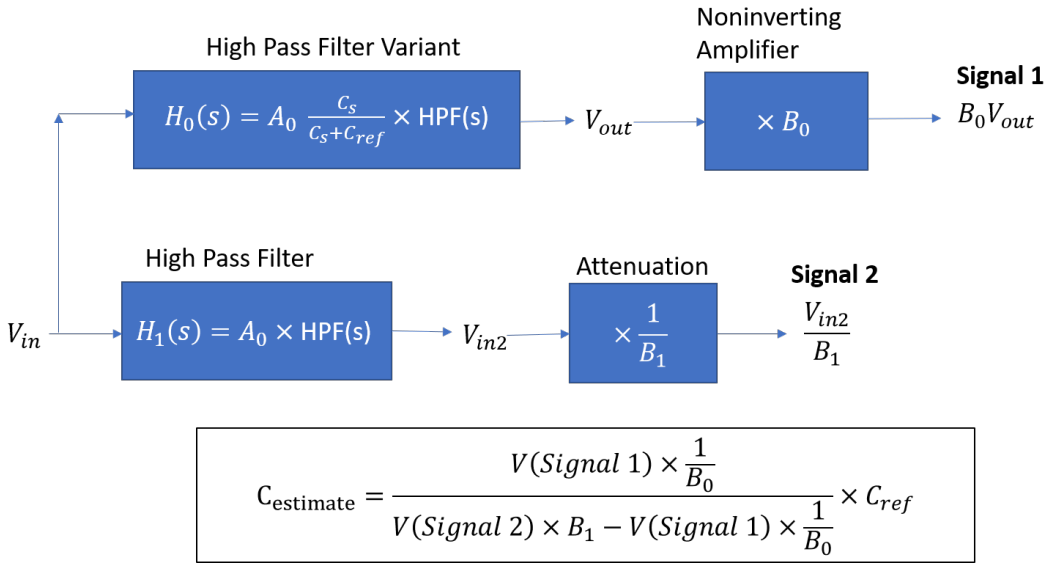


Figure 29: High pass filter amplitude scaling flowchart.

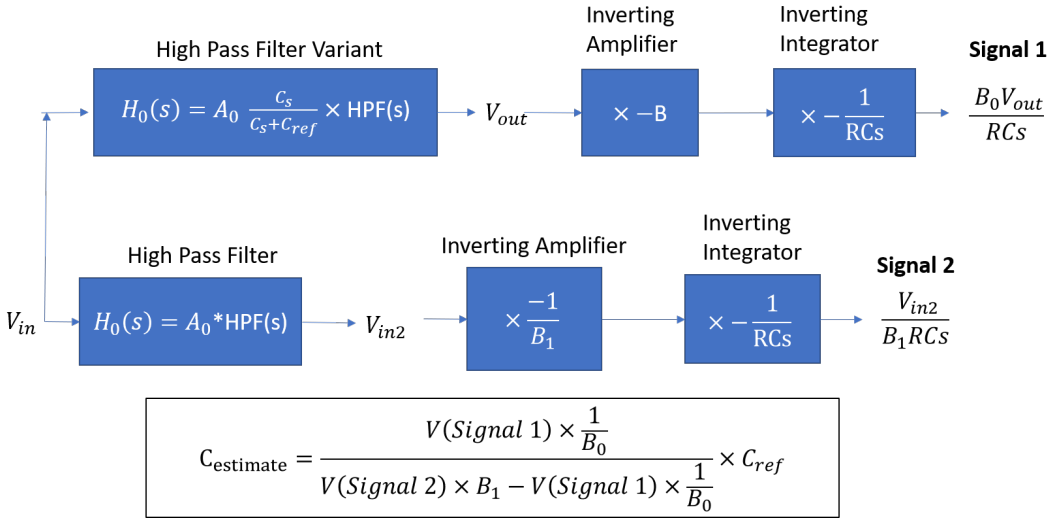


Figure 30: High pass filter amplitude integrating flowchart.

Signal 1 and Signal 2 are scaled in order to fit the input range of any ADC. After this, Signal 1 and Signal 2 analog processing is complete.

Next, the high pass filter integrator flowchart (fig. 30) is explained. Just like before, the Signal 2 path has a high pass filter that matches the high pass filter created in the high pass filter variant. Next, like the integrator case for the all pass filter, the circuit is fed into an inverting amplifier and an inverting integrator. This

completes the processing of the Signal 1 and 2.

In the end, both designs provide two signals that can be used to estimate the capacitance of the capacitor. For both designs, they use slightly different equations to estimate the capacitance. Instead the equations are as follows.

$$V_{\text{out}} = \frac{V(Signal1)}{B_0} \tag{8}$$

$$V_{\text{in2}} = \frac{V(Signal2)}{1/B_1} \tag{9}$$

$$Cs = \frac{V_{\text{out}}}{V_{\text{in2}} - V_{\text{out}}} \times Cref \tag{10}$$

After designing the signal blocks, the next step is to design the circuit that will emulate the signal processing block as seen in Figures 31 and 32. The gain values of both circuits are shown in the Table 3. One important constraint for the high pass variant analog processing circuit is that the selection of the filter capacitor for Signal 2 has to have the same capacitance as sum of Cref and Cs. This is because the sum determines the corner frequency and discharge time of DC offset in the high pass filter variant. By mimicking these properties, Signal 2 will be able to respond in step with Signal 1.

When combining the signal processing circuit, the complete circuit models for the amplitude scaling circuit and the amplitude integrating circuit are obtained and can be found in Figures 64 and 65 in Appendix A. This can then be used to run a complete

Table 3: High Pass Filter Circuit Gain Values

Circuit	$\mathbf{B_0}$	$\mathbf{B_1}$
Scaling	11	2
Integrating	10	1

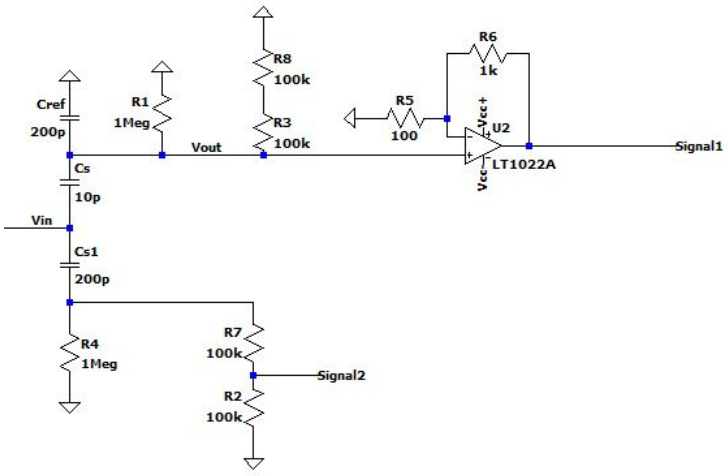


Figure 31: High pass filter amplitude scaling circuit.

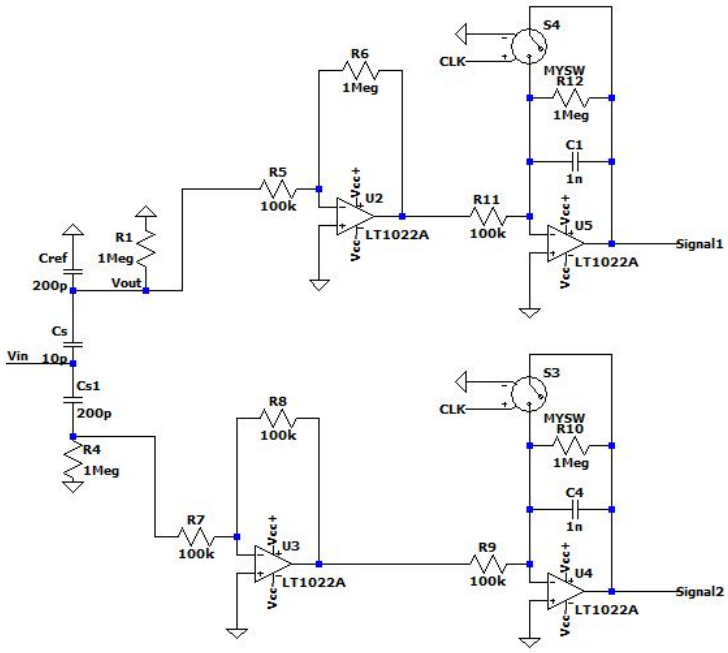


Figure 32: High pass filter amplitude integrating Circuit.

simulation of the whole system. After verifying the signal processing circuit simulation produces the intended output signals and is able to estimate the capacitance of the MEMS, the next step is to experimentally test the complete circuit. For this system, testing will be done where the varying factors will only be the amplitude and the

pulse width. In order to verify if the circuit works as expected, the capacitance of the device will be compared with the capacitance of the system. This concludes the methodology section.

IV. Results and Analysis

4.1 Preamble

In this section, results obtained from the methodology section will be analyzed and discussed.

4.2 Preliminary Test Results and Analysis

The first set of results analyzed was the data from the ideal circuit simulation. These results will give the general feel of what kind of output can be expected when working with such a system. As seen in Figure 33, when a PWM signal is passed through the ideal capacitor divider circuit, a PWM drive signal that has a fraction of the input signal is created. This fraction should be equal to the capacitance of the top capacitor, 20 pF, divided by the total capacitance added together, 220 pF, which is around .091. This is in agreement with the ratio of the V_{in}, 5 V, to V_{out}, .45454 V, which is also .091.

The next set of results analyzed was to verify that a change in capacitance can

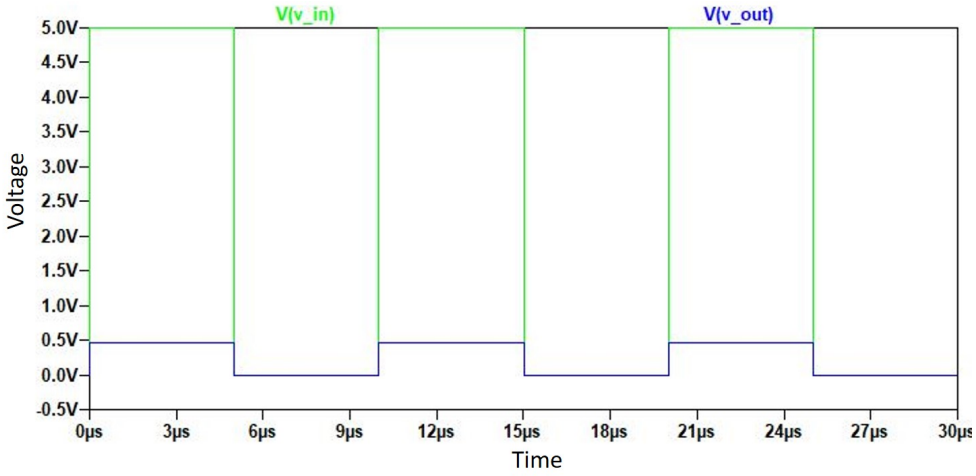


Figure 33: LTspice® simulation data of the ideal capacitor divider circuit. Blue line represents V_{in} and the green line represents V_{out}.

Table 4: R Studio output of ANOVA test ran on preliminary data using $\alpha = .05$.

Factor	**F value**	**PR(<F)**
Trimmer Position	379.714	<2e-16
Duty Cycle	0.865	0.357
Trimmer Position:Duty Cycle	0.000	0.998

be measured in a capacitor divider circuit using square waves. Table 4 shows the F value output obtained from analyzing the data using R. With an alpha value of .05 we can reject the hypothesis that there is no difference in the capacitance estimated due to a change in the trimmer position with a p value of <2e-16. This shows that the variations of voltage measurements obtained align with changes in the trimmer capacitors position, which for a trimmer capacitor means a change in capacitance. This is helpFul because it gives confidence that the capacitor divider circuit can be used to detect a change in capacitance and verifies previous work completed.

4.3 Drive and Interface Circuit Test Analysis

4.3.1 PWM Drive Results and analysis

The next section to be analyzed is the PWM drive circuit simulation and experimental data. For this section, the desired output is the PWM drive signal. The first set of results compared is the simulated and experimental data produced after the MOSFET Driver is connected to the waveform generator. As can be seen in Figures 34 and 35, both the simulation and experimental data have the same shape: ringing after the rising and falling edges and a hump at the end of the on cycles. Although the ringing is more significant in the experimental data, this is acceptable because it can be due to the discrepancies in the real components and the ideal. Also, as long as ringing is present in the simulation it can be used as an indication that ringing will occur at certain locations in the signals. Ultimately, they both produce basically the

same shape of the desired PWM signal. With this we can proceed to the next step in building the system.

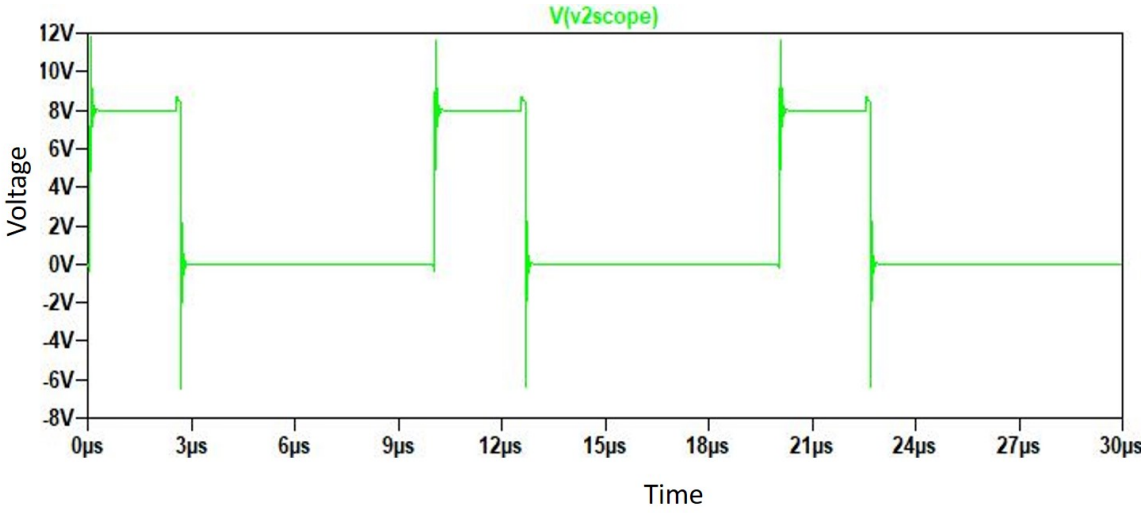


Figure 34: LTspice® Simulation data of the MOSFET driver circuit.

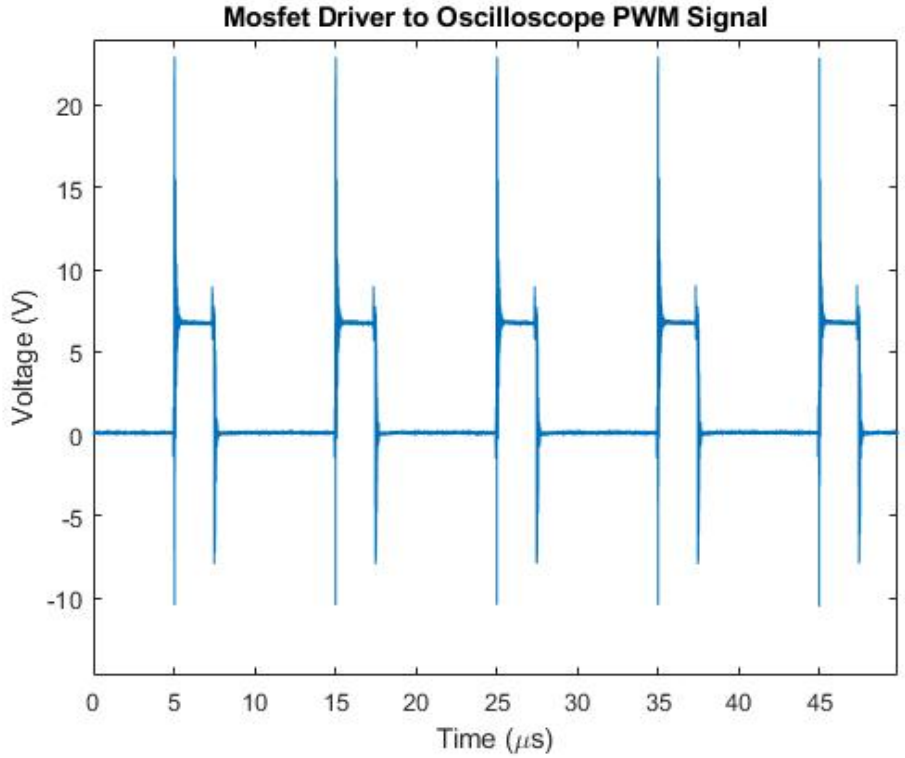


Figure 35: Experimental data of the MOSFET driver Circuit.

4.3.2 Interface Circuit Results and Analysis

The next system analyzed is the complete system which includes the signal generator, MOSFET driver, the interface circuit, and the capacitor divider circuit. The end goal of this circuit is to produce two output signals, V_{in}, which is the input PWM signal, and V_{out}, which is the voltage divided output PWM signal. As can be seen in the simulation data, Figure 36, the data shows that the output signals obtained in the simulations for V_{in} and V_{out} are of the desired form. The V_{in} signal produces a PWM signal with the correct amplitude and frequency. The V_{out} signal produces PWM signal with the same frequency but its amplitude is a fraction of the V_{in} signal.

However, in the experimental case, not all the signals come out correctly. Although the experimental V_{in} signal data seen in Figure 37a matches the simulated data, the experimental V_{out} signal seen in Figure 37b data does not match the simulated data. Fortunately, the amplitudes were still able to give adequate capacitance estimates. In the data, V_{in} amplitude obtained is 10 V and the V_{out} amplitude obtained is 600 mV. Using equation 4, this gives an estimated capacitance of 12.2 pF which is close to the actual capacitance of 10 pF. Despite this success, the problem with the data is that the signal shifts down to a new equilibrium about zero, which is not displayed in

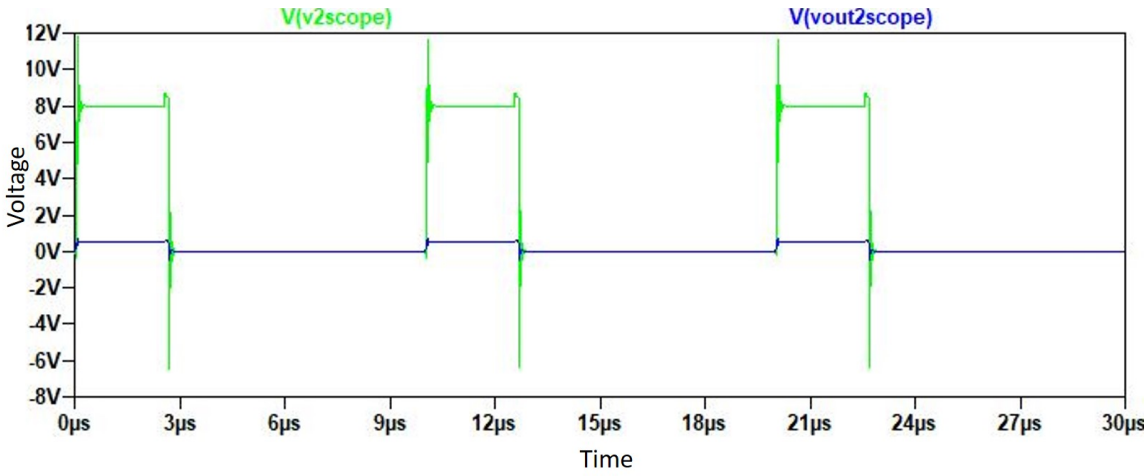
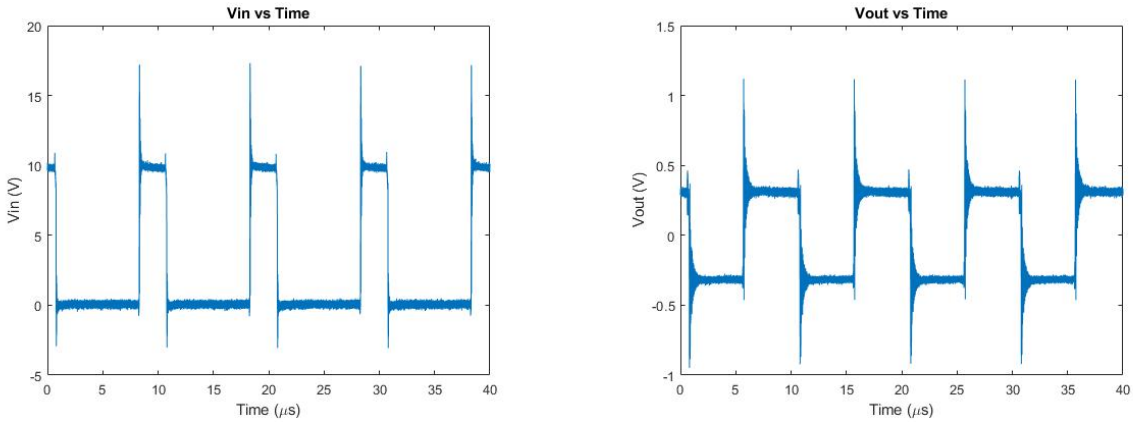


Figure 36: Simulation V_{out} and V_{in} Signals.

the simulated output. This occurs at all the different duty cycles as shown in Figure 38.

Next, the reason for the difference between the simulated and experimental outputs needs to be identified. PWM signals in general are a sum of a DC offset and a combination of AC Signals. It appears as though, the DC component of a PWM



(a) Experimental data for V_{in}. (b) Experimental data for V_{out}.

Figure 37: Sense circuit outputs

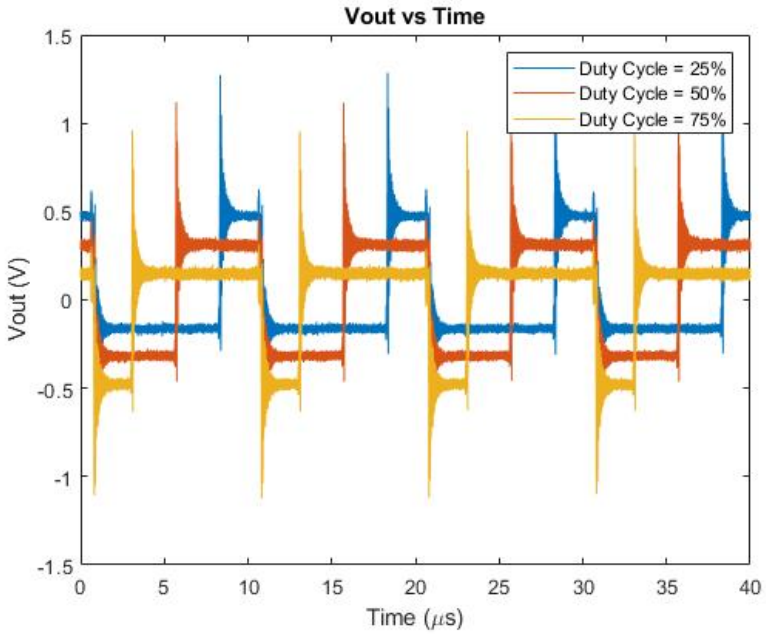


Figure 38: Experimental data for V_{out} at different duty cycles.

signal is filtered out of the device. First, what was not included in the first take was the transmission line connection to the oscilloscope. After looking at the circuit in a more simplified approach as in Figure 39, it becomes apparent that a high pass filter is created. This then filters out the DC component of the PWM signal from the V_{out} signal. The high pass filters is created when the oscilloscope is connected to the midpoint of the capacitor divider circuit. When the oscilloscope is connected to the circuit it adds additional impedance components, that need to be accounted for.

As can be seen in this Figure 40, over time the output signal slowly shifts downwards until it reaches its steady state. During this transition phase, the DC signal is filtered out and the signal moves towards an equilibrium where the integral of one period equals zero. Since this process is not instant, a good amount of time, around 0.8 ms, needs to pass before reaching steady state.

With this information the correct LTspice® circuit needs to contain the oscilloscope and also needs to run for a long period of time before reaching steady state. Since the simulation takes a while to run, a snapshot starting a 70 microseconds was run in order to show that the signal was shifting down. As can be seen in figure 41 the output signal shifts downwards which is in line with what was observed in the experimental results.

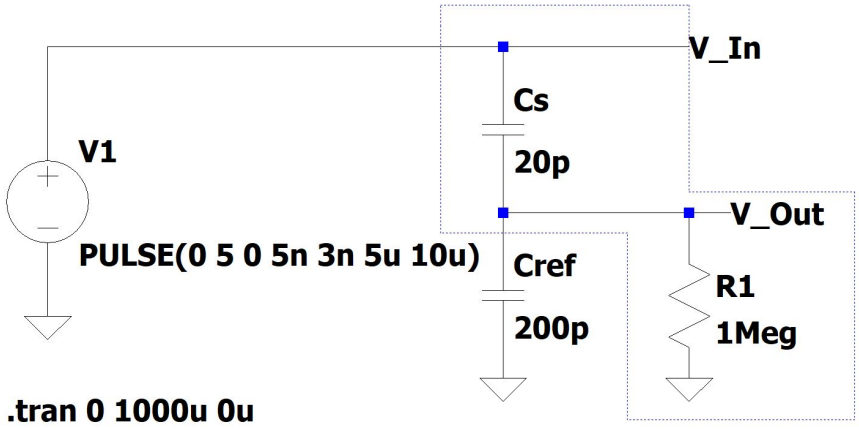


Figure 39: High pass filter created by parallel resistance.

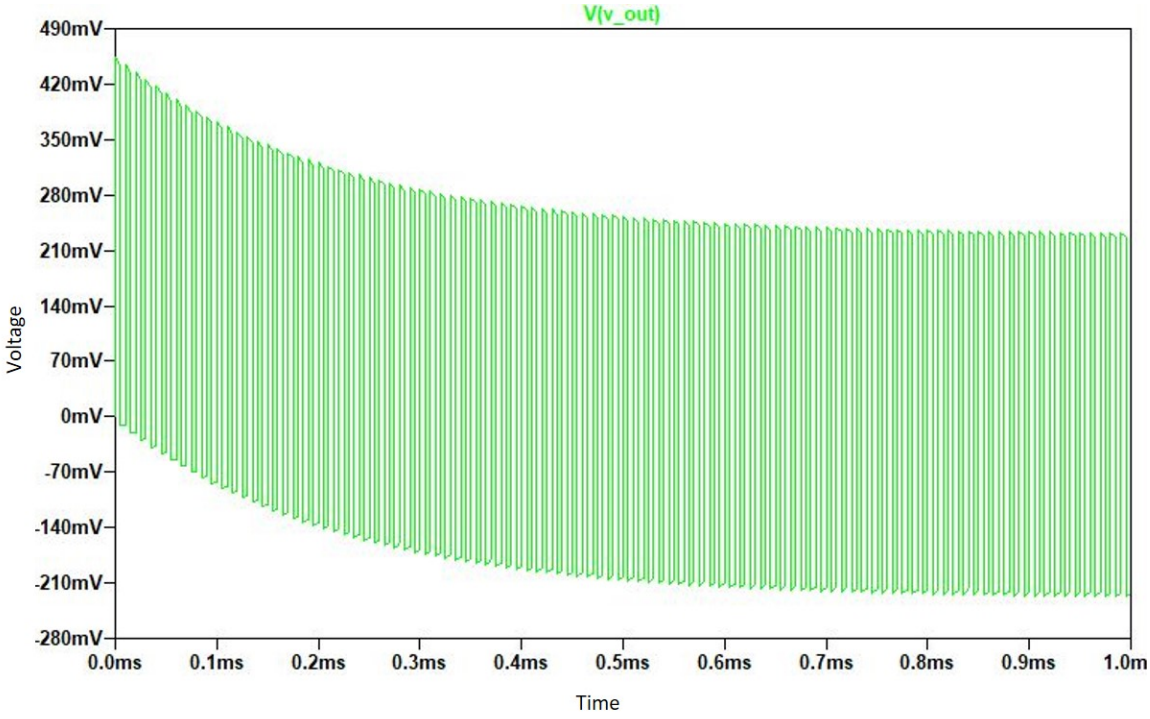


Figure 40: Ideal high pass filter simulation over 1 ms.

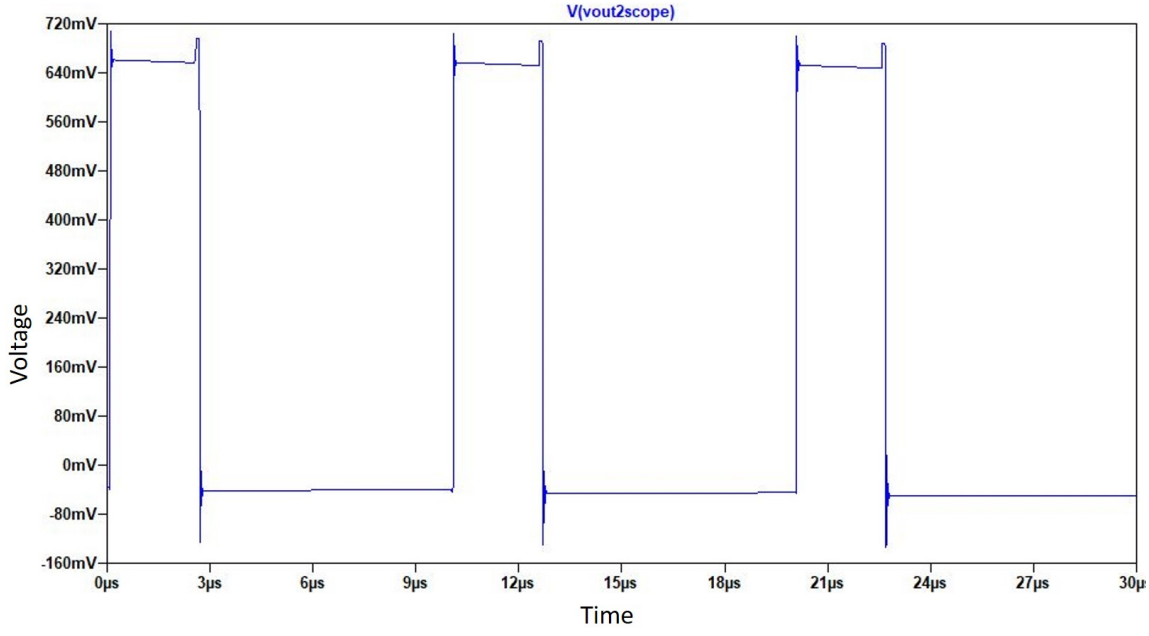


Figure 41: V_{out} after 75 microseconds.

From this analysis, we learn two important characteristics. First, when trying to measure the output of the signal any non-capacitive parallel impedance will create

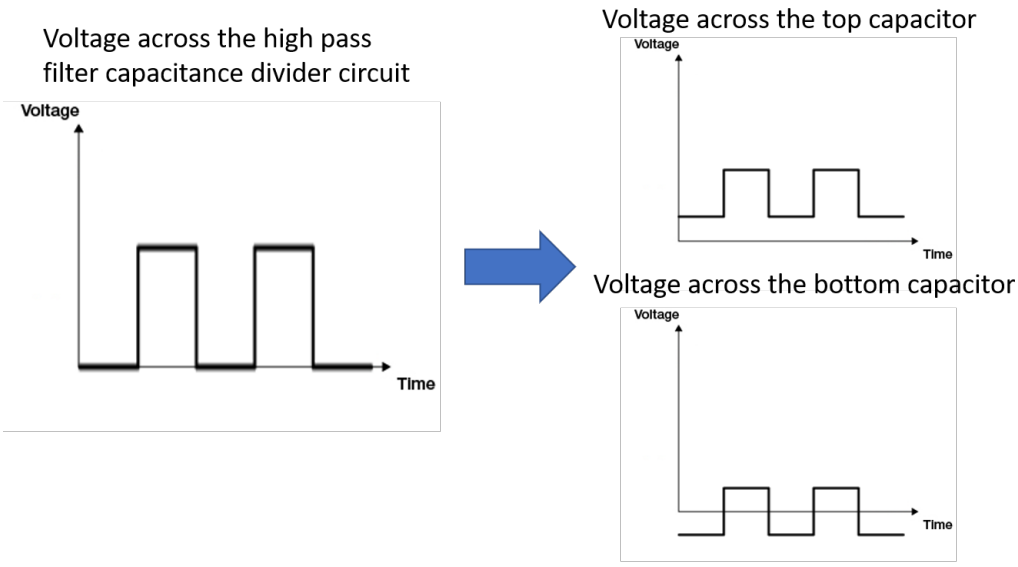


Figure 42: The effect of the High Pass Filter on the voltage signals across capacitors after stabilization.

a high pass filter that will filter out the DC bias from the bottom capacitor once the system stabilizes. After stabilization, two different signals across the two series capacitors are created. As shown in Figure 42, the voltage signal across the bottom capacitor stabilizes about zero where the DC bias is filtered out. On the other hand, the voltage across the top capacitor is a combination of two signals, the regular PWM signal without the high pass filtering plus the DC component that was filtered out of the bottom capacitor. The DC offset also varies with the duty cycle. The relationship is that as the duty cycle increases, the DC offset increases as well. Since the DC offset changes with duty cycle, this adds variability to the control scheme. However, in the case of actuation, it is preferable to provide more force during higher duty cycles than lower. The DC offset being greater in higher duty cycles helps to ensure that the actuation force is greater as well. Also, when the capacitance ratio (Cs/Cref) is significantly small, then DC variation due to the duty cycle becomes negligible. As a result, the placement of the electrostatic MEMS actuator matters because it will

effect what kind of signal is applied to it. In the case where the actuator is placed on the top of the interface circuit, the signal applied to the actuator will have a voltage during its on and off cycles. However, due to the requirement that capacitance ratio (Cs/Cref) is significantly small, the amount force generated during its off cycle is significantly smaller than during its on cycle. As a result, the voltage during the off cycle will have less and potentially negligible influence on the actuation of the device. On the other hand, in the second case, where the actuator is placed at the bottom of the series connection, there is less of a contrast between the voltages during the on and off cycles. This is because a negative voltage across the electrostatic MEMS actuator will have the same force as a positive voltage across the electrostatic actuator. As a result, the on and off cycles will both have a significant effect on the electrostatic MEMS actuator. Another interesting phenomenon in this case is that the on and off voltages fluctuate based on the duty cycles when the capacitance ratio is not small. The duty cycles end up having a combination of (100-x)% of the amplitude of V_{in} during the on time and x% of the amplitude of V_{in} during the the off time, where x is the duty cycle. For example, if the duty cycle is set to 25% then the voltage during the on time is 75% of the total amplitude and the voltage during the off time is 25% of the total amplitude. With all this information, it would be prudent to have the electrostatic MEMS actuator be the top capacitor in the high pass filter variant of the capacitor divider circuit as it reduces variability of the control signal across the capacitor.

The next information inferred about this circuit is that the response time of the sensing circuit is increased by the introduction of a parallel resistance. As seen earlier, some time needs to pass before the circuit can filter out the DC signal and stabilize. In general the time it takes to stabilize the system is around the slowest RC time constant of the high pass filter (which in this case is 1 MOhm times 200 pF) 2 microseconds. A

smaller time constant, due to a smaller resistance, means a quicker stabilization time. A bigger time constant, due to a larger resistance, produces a slower stabilization time. If a quick stabilization of the circuit is desired a small resistance can be used; however, the size of the resistor will also affect what frequencies are allowed to pass. If the resistor is too small, the high pass filter's corner frequency can be too high and their is a possibility that the drive signal could be filtered out as well. As a result, the drive signal would be required to have a higher frequency which is not an issue, as higher frequency signals are generally more desirable. Lastly, this signal takes advantage of the leakage problem described in reference [30]. Instead, the leakage is used to remove the DC offset and create a high pass filter variant. This configuration of the capacitor divider is a viable option as an interface circuit as sense capacitance can still be estimated from the amplitude of the output signal.

Ultimately, this leads to two distinct variations of the capacitor divider circuits as seen in Figure 23 in chapter III section 3.5.3: the high pass filter variant and the all pass filter variant. The high pass filter is the capacitor divider with a parallel resistance as previously explained. This variant would require a circuit that finds the amplitude difference between the on and off cycles. The all pass variant of the capacitor divider circuit is where the voltage follower circuit with a large enough input impedance (effectively infinite) is used to sample the circuit V_{out} and is the traditional approach. This allows for DC offset to not be filtered out of the system and produces a regular PWM signal across both the top and bottom capacitors. In this case, the electrostatic MEMS actuator can be on the top or bottom. It is recommended that the actuator be the top capacitor as it would allow for a lower output voltage.

4.4 Signal Processing Results and Analysis

Next, the complete circuit with the signal processing block was simulated and physically tested. In this section, the all pass filter variant performances will be analyzed first in both the amplitude scaling circuit and the amplitude integrating circuit cases. One important thing to point out is that the variable capacitor, Cs, used was a trimmer capacitor varied between two capacitance values, 14 pF (Cs 1) and 7 pF (Cs 2). The constant parameters used in in all experiments are in Table 5. It is also important to remember that Signal 1 is the output generated from V_{out} and Signal 2 is the output generated from V_{in}.

4.4.1 All Pass Filter Analysis

4.4.1.1 Amplitude Scaling Circuit Analysis

In the all pass filter case the amplitude circuit is first analyzed. Figure 43 shows the output obtained after running the LTspice® simulation on the amplitude scaling circuit. The graphs show PWM signals outputs for V_{in} and V_{out} with different amplitudes. This is good because a capacitor divider circuit divides the voltages across the capacitors that are scaled differently. In order to verify that the simulation performed as intended, a data point at a certain point in time can be selected from both signals to estimate the capacitance. For example, at time 15 microseconds, V(signal1) equals

Table 5: Drive and interface circuit parameters.

Initial Variable	**Value**
PWM amplitude	10 V
PWM Frequency	100 kHz
Cref	200 pF
Cs 1	14 pF
Cs 2	7 pF

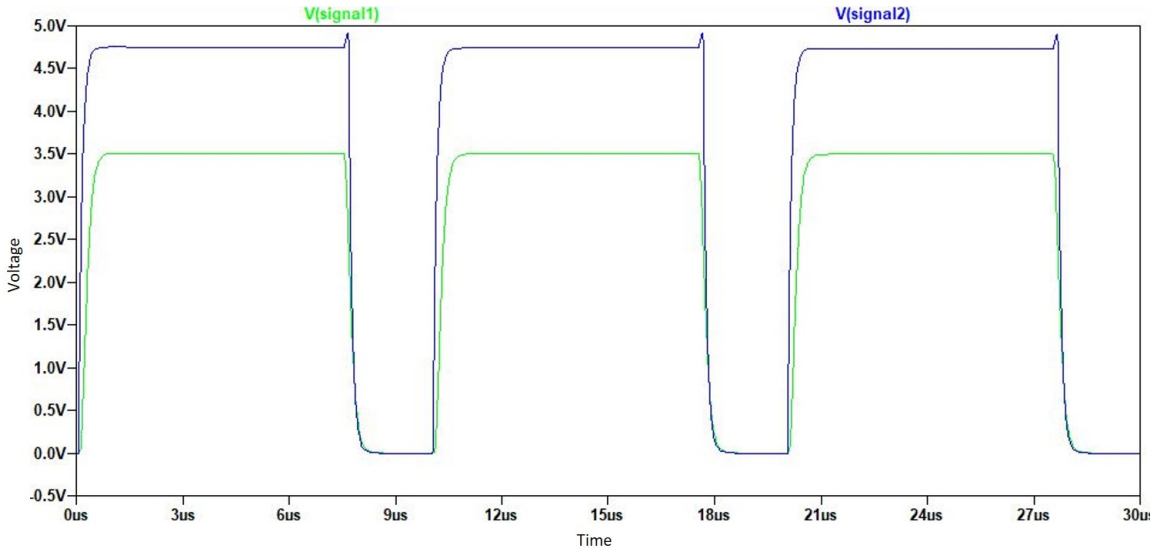


Figure 43: Signal 1 and Signal 2 simulation output for the all pass filter amplitude scaling circuit.

3.50 mV and V(signal2) equals 4.74 mV. Using equations 5, 6, and 7 and the circuit gains (B_0=5.7 and B_1=2), the estimated capacitance obtained is computed as 13.85 pF. This is very close to the actual capacitance in the simulation of 14 pF. This difference can possibly be due to the nonideal circuit models, like the manufacturer opamp models, used. The simulation shows that this circuit can estimate the capacitance of the sense capacitor.

With confidence in the output from the simulation of the circuit design, the experimental circuit was next tested. Figures 44, 45, and 46 show graphs of the output voltage from Signal 1 and Signal 2. At first, the signals received are shaped as PWM signals with the same amplitudes independent of of duty cycles. However, their are many non-idealities present. First, in Signal 1 there seems to be a superimposed sinusoidal signal during the on cycle. This could be attributed to vibrations in the room, the feedback of the noninverting opamps trying to keep the inputs at the same voltage, or the perturbations in the rail voltages that are shared by many opamps. The second is the sharp spikes that occur at the edges of the on and off cycles. These

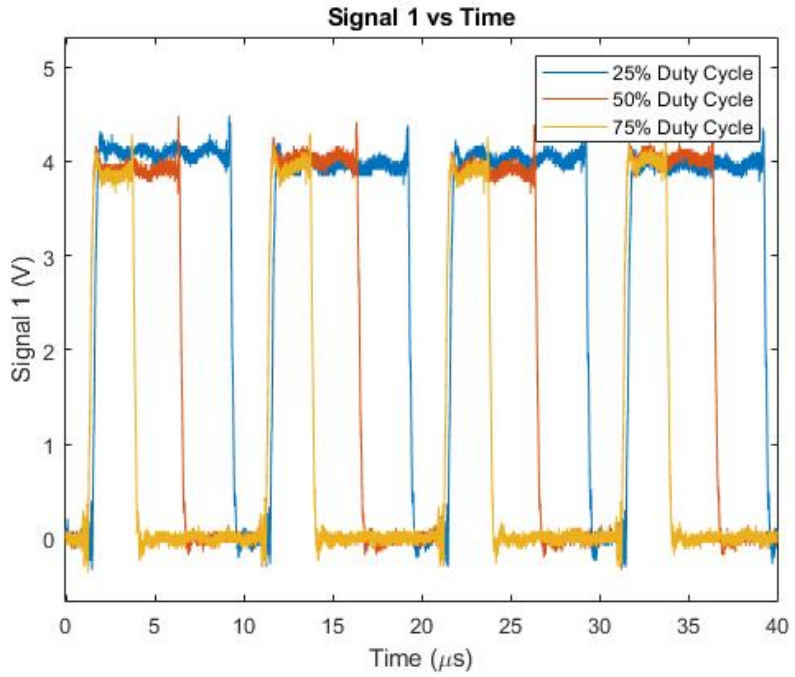


Figure 44: Amplitude circuit Signal 1 output when Cs is 14 pF.

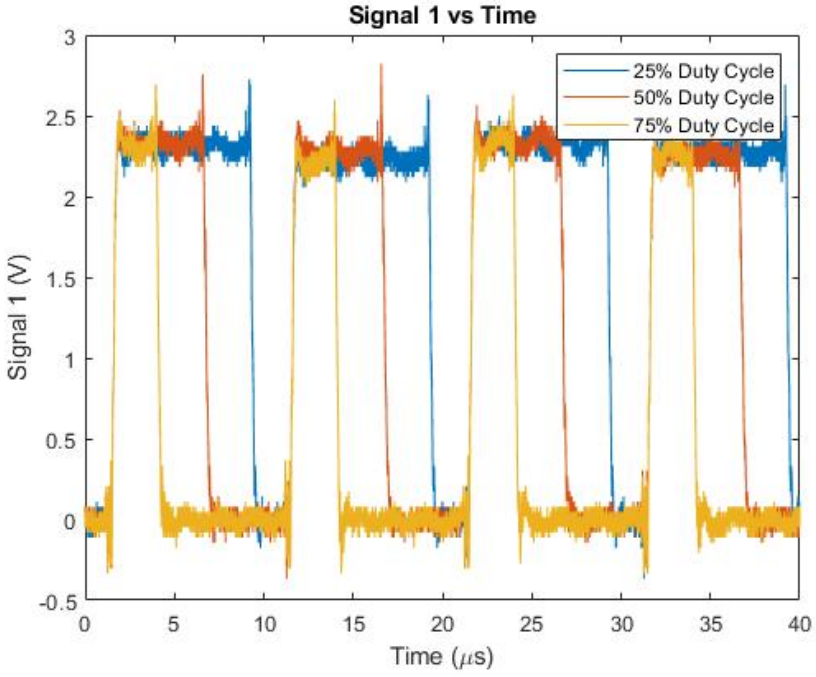


Figure 45: Amplitude circuit Signal 1 output when Cs is 7 pF.

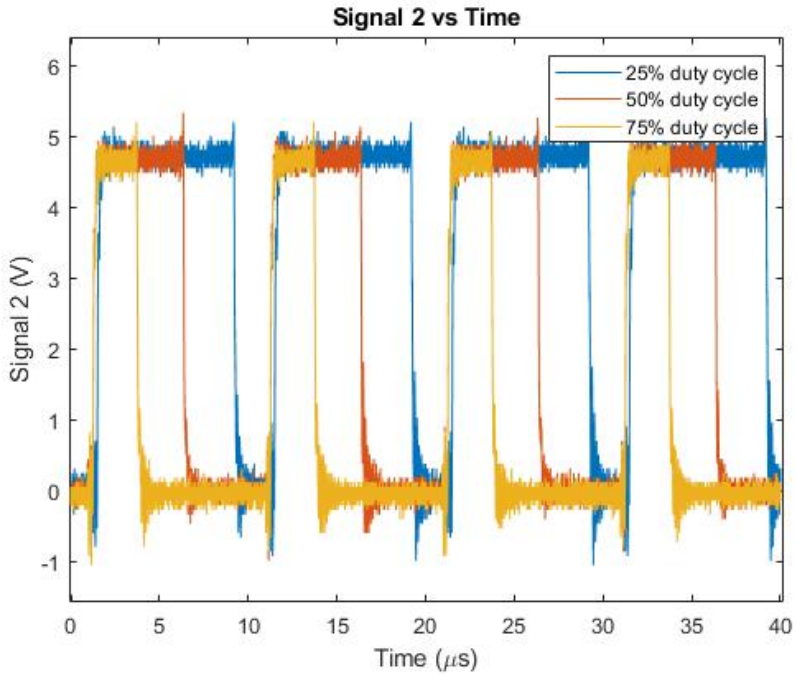


Figure 46: Signal 2 output.

sharp rings are typical of switching due the MOSFETs and the reset signal switch. Lastly, the amplitude varies slightly over each period. This error is most likely due to noise in the measurements and environment as well. Arguably the most important verification step is to verify if estimations come out close to the sense capacitance (Cs) values.

From the data, the output voltages are sampled periodically over 200 microseconds and analyzed in MATLAB®. This results in 20 samples. Table 6 shows the obtained

Table 6: Amplitude scaling circuit capacitance estimates.

Cs (pF)	DC	$\mathbf{A_0}$	$\mathbf{B_0}$	$\mathbf{A_1}$	$\mathbf{B_1}$	$\overline{\mathbf{Cest}}$ **(pF) (n = 20)**	**Std Dev (pF)**
14	75	0.952	5.7	0.952	2	16.150	.419
14	50	0.952	5.7	0.952	2	16.026	.421
14	25	0.952	5.7	0.952	2	15.864	.349
7	75	0.952	5.7	0.952	2	8.855	.291
7	50	0.952	5.7	0.952	2	9.020	.295
7	25	0.952	5.7	0.952	2	9.171	.315

capacitance estimate when the output data and the gain constants are plugged into equations 5, 6, and 7. Overall, the estimates are close estimates of the sense capacitance and are off by one to two picofarads. The error is caused by parasitic capacitances that are in parallel with the capacitors which introduce voltage offsets. This can be from the breadboard, long wires, and electromagnetic interference. Despite these errors, the amplitude scaling circuit is capable of measuring changes in capacitance. Overall, the amplifier circuit shows that it has potential to be used for feedback control.

4.4.1.2 Amplitude Integrating Circuit Analysis

Unlike the amplitude circuit, the integrator circuit works by integrating the input voltage signals over one or multiple integration periods. If the integrator integrates over multiple periods, the voltage output can be divided by the number of cycles in order to give an averaged value. This reduces the variability that occurs between samples because it takes the average of multiple samples. However, this also slows

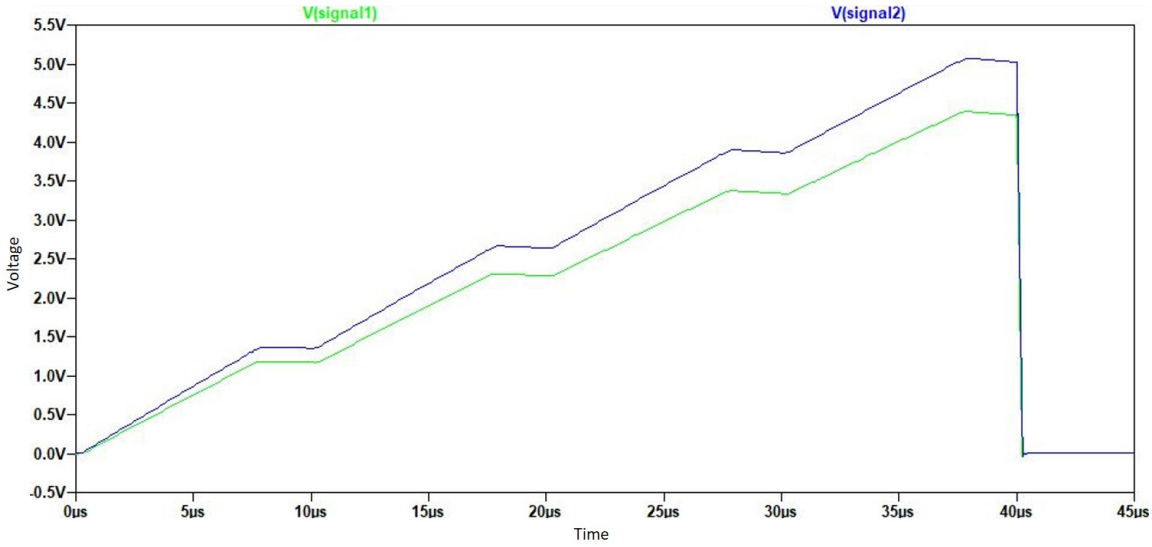


Figure 47: Signal 1 and Signal 2 simulation output for the four integration periods circuit.

the sampling rate as it takes more time to sample over more periods. Figure 47 shows the output obtained after running the simulation on the integrator circuit integrating over four periods. In order to estimate the capacitance, voltage samples were taken at time 39.40678 microseconds. At this time, the voltage of Signal 1 is 4.367 mV and the voltage of Signal 2 equals 5.049 mV. Using equations 5, 6, and 7, the estimated capacitance obtained is 14.78 pF. This is close to the actual capacitance in the simulation of 14 pF. This difference can possibly be due to the nonideal circuit models, like the manufacturer opamp models, used. The simulation shows that this circuit can give a close estimate the capacitance of the sense capacitor. The next step is to experimentally test the circuit.

First, the one integration period case was observed. The output voltages are shown in Figures 48, 49, and 50. As seen in the figures, signals give the correct shape outputs. The signals shape is a line with a constant positive slope during the on cycles and a constant zero slope during the off cycles. The spikes present in the signal are

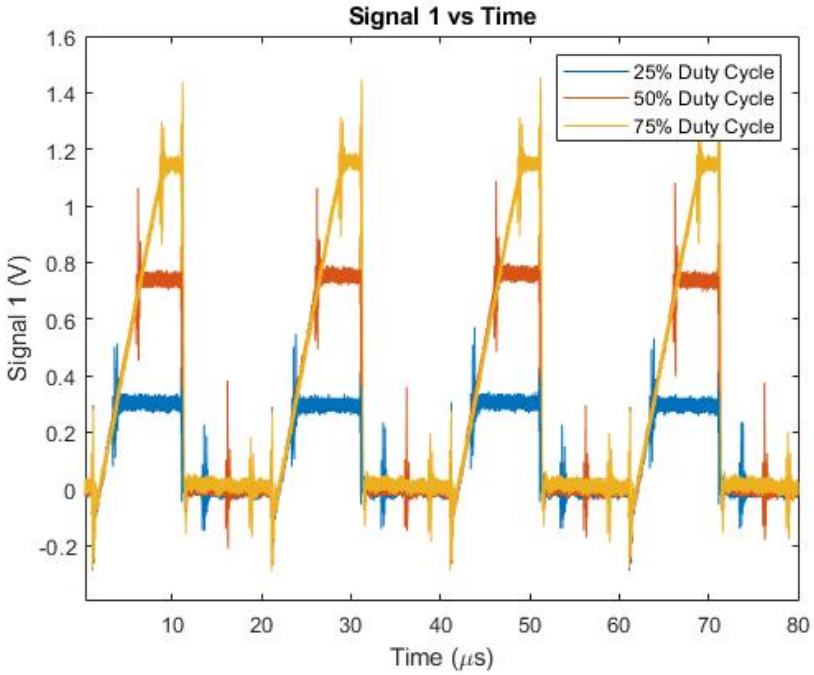


Figure 48: One integration period Signal 1 output when Cs is 14 pF.

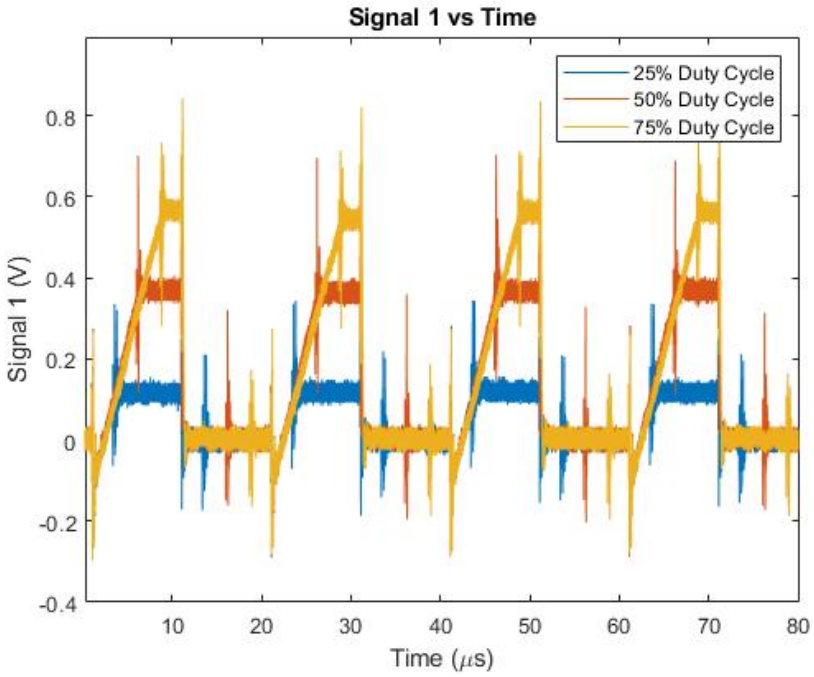


Figure 49: One integration period Signal 1 output when Cs is 7 pF.

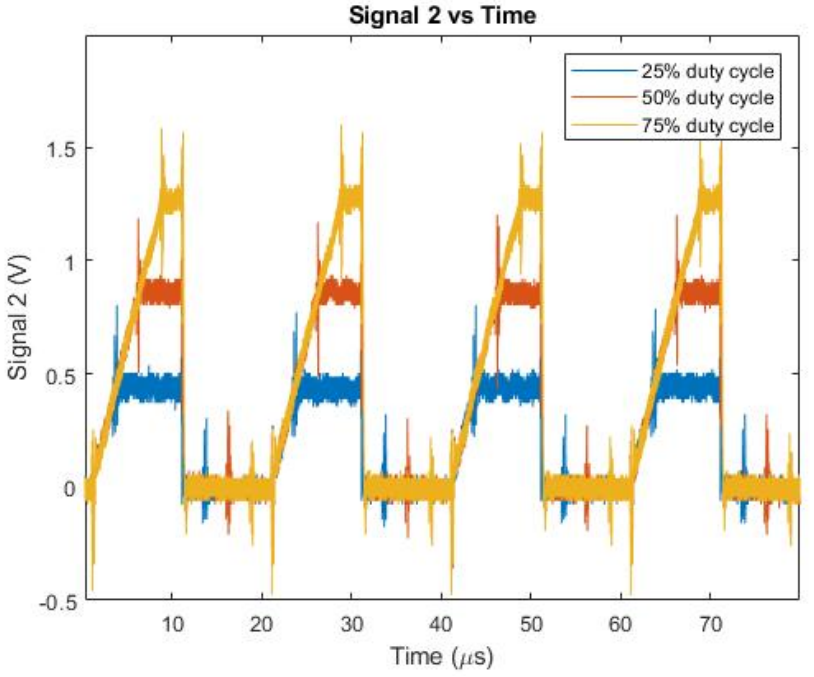


Figure 50: One integration period Signal 2 output.

due to the switching of on and off duty cycles and the switching of the reset signal of the integrator. The last main nonideality found in the data is that the Signal 1 starts integrating from around -0.06 V instead of zero volts. This exists in Signal 2 but is not as visible. This seems to be due to some parasitic capacitor that is negatively charged while the integrator is in its off state. As a result, when the reset signal is turned on the integrating capacitor is immediately negatively charged. This could also be due to the nature of an opamp to try and keep the negative input close the positive input and subsequently causes charge to flow into the capacitor. The next step is to compare the sense capacitance (Cs) estimates from the signal.

From this data, the output voltages are sampled periodically over 200 microseconds and analyzed in MATLAB®. This results in 10 samples which means the sampling period has doubled compared to the amplitude circuit. Table 7 shows the obtained capacitance estimate when the output data and the gain constants are

Table 7: One integration period capacitance estimate.

Cs (pF)	DC	$\mathbf{A_0}$	$\mathbf{B_0}$	$\mathbf{A_1}$	$\mathbf{B_1}$	$\overline{\textbf{Cest}}$ **(pF) (n = 10)**	**Std Dev (pF)**
14	75	0.5	10	0.99	0.37	14.223	.534
14	50	0.5	10	0.99	0.37	13.079	.512
14	25	0.5	10	0.99	0.37	10.347	.772
7	75	0.5	10	0.99	0.37	5.794	0.144
7	50	0.5	10	0.99	0.37	5.071	0.109
7	25	0.5	10	0.99	0.37	2.634	0.112

Table 8: One integration period capacitance estimate compensated.

Cs (pF)	DC	**Comp.** $\overline{\textbf{Cest}}$ **(pF) (n = 10)**	**Comp. Std Dev (pF)**
14	75	15.838	0.541
14	50	15.449	.545
14	25	14.995	0.987
7	75	7.271	0.174
7	50	7.281	0.141
7	25	6.904	0.203

plugged into equations 5, 6, and 7. The first major issue that appears is that each duty cycle gives a different estimate by one to four picofarads. Furthermore, many of the estimates are entirely wrong. The signals that give the worse estimate are the signals with the smallest duty cycles and smallest final voltages. This is undesired because, regardless of duty cycle, the estimates should be around the same value. This error could be caused by the negative offset that occurs at the start of the integration cycle. When subtracting the -0.06 V offset, the estimates do become better as can be seen in Table 8. The estimates are closer in range to each other and also give a more accurate estimate of the sense capacitances (Cs) in both the on and off cycles. This outcome is reasonable as it shows that the voltage offset has less of an effect on larger signals.

Next, the multiple integration periods circuit data was investigated. Figures 51, 52, and 53 shows the voltage output of Signal 1 when Cs is 14 pF and 7 pF and Signal 2, respectively. As seen in the figures, the signals give the correct shaped outputs. The signals shape are four single integration periods steps stacked edge to edge. This signal has the same nonidealities, the voltage spikes and negative voltage offset are present. The next step is to compare the sense capacitance (Cs) estimates from the signal.

From this data, the output voltages are sampled periodically over 200 microseconds and analyzed in MATLAB®. This results in four samples which means the sampling period has increased by five compared to the amplitude circuit. Table 9 shows the obtained capacitance estimate when the output data and the gain constants are plugged into equations 5, 6, and 7. Overall, the estimates are close to the set sense capacitance values. The error is caused by parasitic capacitances that are in parallel with the capacitors which introduce voltage offsets. Furthermore, as the duty cycle changes, the mean estimates are relatively close to each other. Despite these

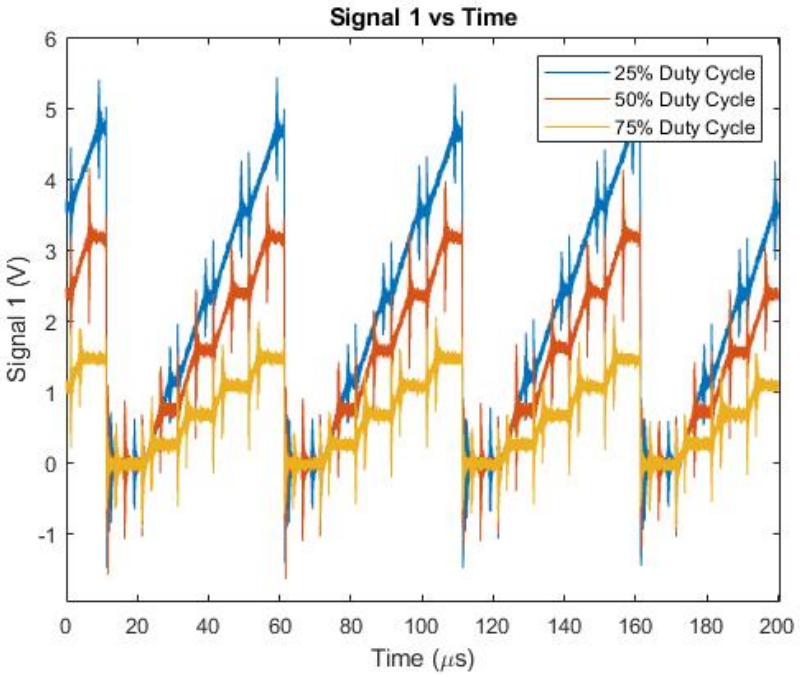


Figure 51: Four integration periods circuit Signal 1 output when Cs is 14 pF.

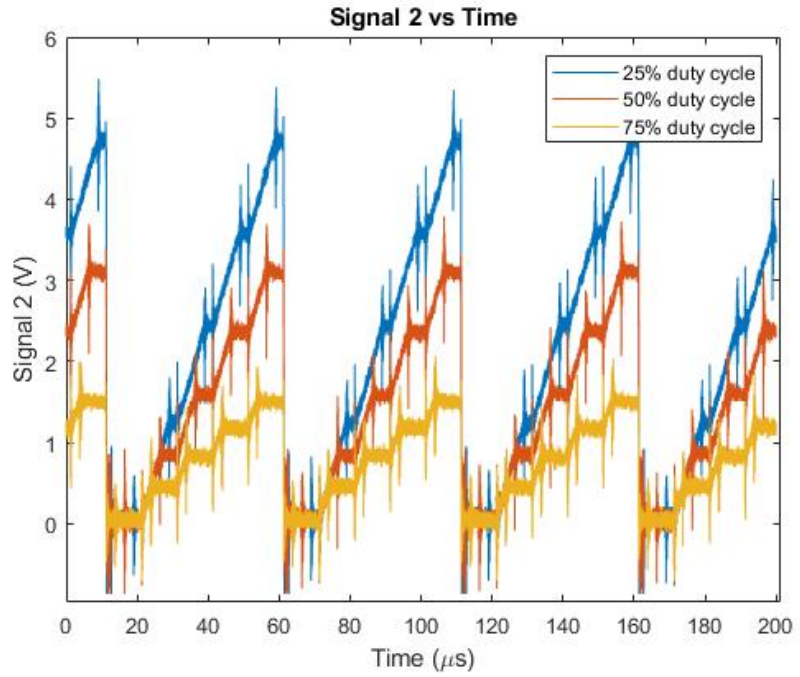


Figure 52: Four integration periods circuit Signal 1 output when Cs is 7 pF.

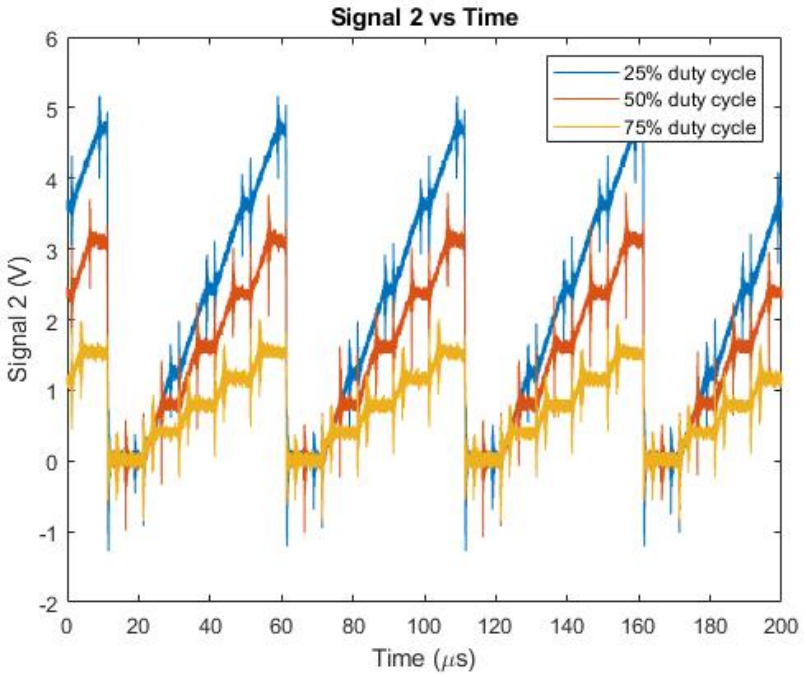


Figure 53: Four integration periods circuit Signal 2 output.

errors, the amplitude scaling circuit tracks the changes with capacitance with fairly small standard deviation. As a result, the integrator circuit shows that it has potential to be used for feedback of the capacitor. Table 10 shows the obtained capacitance estimate with the initial -.06 V offset compensated. The compensated estimates do not change too much from the uncompensated estimates. This makes sense because since the voltage signals are larger the offset has less of an effect. As a result, the amplitude integrating circuit shows that it can be used for feedback control.

Table 9: All pass filter four integration periods circuit capacitance estimate.

Cs (pF)	DC	$\mathbf{A_0}$	$\mathbf{B_0}$	$\mathbf{A_1}$	$\mathbf{B_1}$	$\overline{\mathbf{Cest}}$ **(pF) (n = 4)**	**Std Dev (pF)**
14	75	0.5	10	0.99	0.37	15.674	.152
14	50	0.5	10	0.99	0.37	16.402	.101
14	25	0.5	10	0.99	0.37	15.674	.366
7	75	0.5	10	0.99	0.37	7.644	.0451
7	50	0.5	10	0.99	0.37	7.527	.225
7	25	0.5	10	0.99	0.37	6.712	.177

Table 10: All pass filter four integration period capacitance estimate compensated.

Cs (pF)	DC	**Comp. $\overline{\text{Cest}}$ (pF) (n = 10)**	**Comp. Std Dev (pF)**
14	75	15.980	.154
14	50	16.375	.105
14	25	16.364	.366
7	75	7.847	.0464
7	50	7.834	.234
7	25	7.33	.189

The four integration periods and one integration period cases differ in the following ways. First, the estimate at 25%, 50%, and 75% duty cycle in the one integration period case were not as consistent as the four integration periods case. This issue seems to be due to a combination of the sense capacitance being small and the duty cycle being low. Another difference between the two cases is that in order to reach the same voltage, if the integration time is shorter, either the larger the amplification needs to be or the integrating capacitor needs to be smaller. An additional important difference is their exists a tradeoff between number of periods integrated and resolution. The trade off is that a greater number of periods integrated gives a better resolution but a slower sampling rate, while a smaller number of periods integrated gives a lower resolution but a faster sampling rate.

Overall, the amplitude and integrator circuits of the all pass variant show good results. The amplitude circuit has the quickest sampling rate but amplifies the errors within the system. For the integrator system, as the number of integration periods increases, the variance decreases and resolution increases. However, the trade off is a slower sampling rate and negative initial offset voltage.

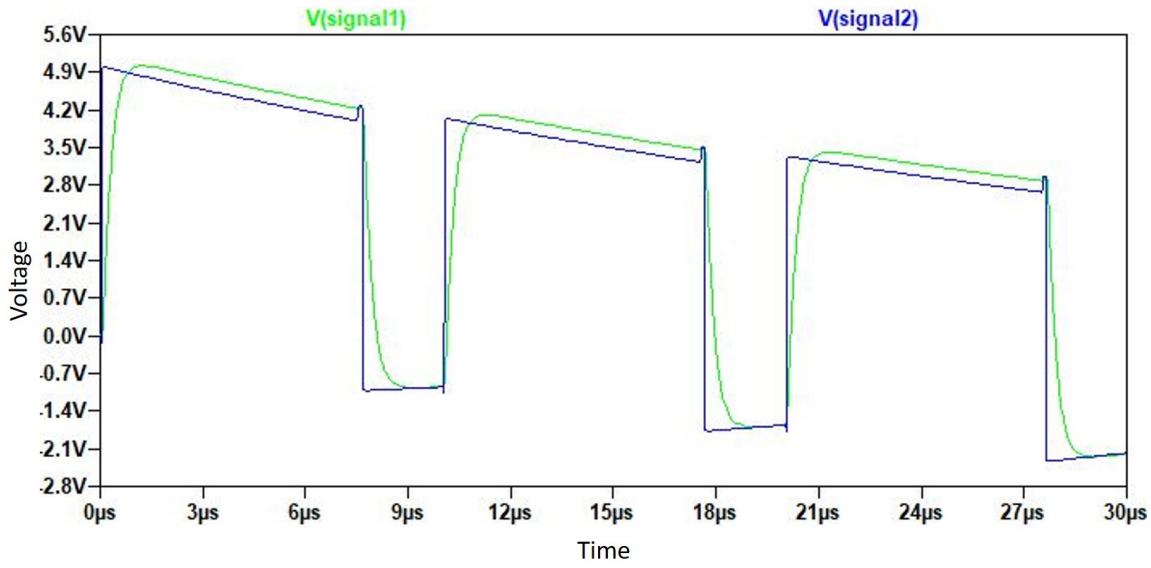


Figure 54: Signal 1 and Signal 2 simulation output for the amplitude scaling circuit.

4.4.2 High Pass Filter Variant Analysis

4.4.2.1 Amplitude Scaling Circuit Analysis

Next, the high pass filter variant is investigated starting with the amplitude scaling circuit. Figure 54 shows the Signal 1 and Signal 2 output obtained after running the LTspice® simulation on the amplitude scaling circuit. Signal 1 and Signal 2 are both PWM signals (Signal 1 has softer edges) that stabilize at the same rate. This is helpFul because it allows the capacitance to be estimated even before the signal is completely stabilized. In order to estimate the capacitance, at time 15 microseconds, voltage was sampled for Signal 1 (3.71 V) and Signal 2 (3.48 V). Using equations 8, 9, 10 and gain parameters ($B_0 = 11$, $B_1 = 2$), the estimated capacitance obtained is computed as 10.185 pF. This is very close to the sense capacitance in the simulation of 10 pF. This difference can possibly be due to the nonideal circuit models, like the manufacturer opamp models, used. As a result, the simulation shows that this circuit should perform well enough to estimate the capacitance of the sense capacitor.

With confidence in the output from the simulation of the circuit design, the exper-

imental circuit was tested. Figures 55, 56, and 57 show graphs of the output voltage from Signal 1 when Cs is 7 pF and 14 pF and Signal 2, respectively. The outputs from Signal 1 and Signal 2 are PWM shapes about zero. This means that the signals have their dc component blocked off. Overall the signal does a great job in maintaining stability. As usual their is some spiking due to switching of the transistors, but overall the signal is quite consistent with the simulation output.

From this data, the output voltages are sampled periodically over 200 microseconds and analyzed in MATLAB®. This gives 20 samples. Table 11 shows the obtained capacitance estimate when the output data and the gain constants are plugged into equations 8, 9, and 10. Overall the estimates at each duty cycle are quite consistent and give estimates that are close to the measured sense capacitance values of 14 and 7 picofarads. The difference could be due to either incorrect trimmer capacitance position or parasitic capacitances.

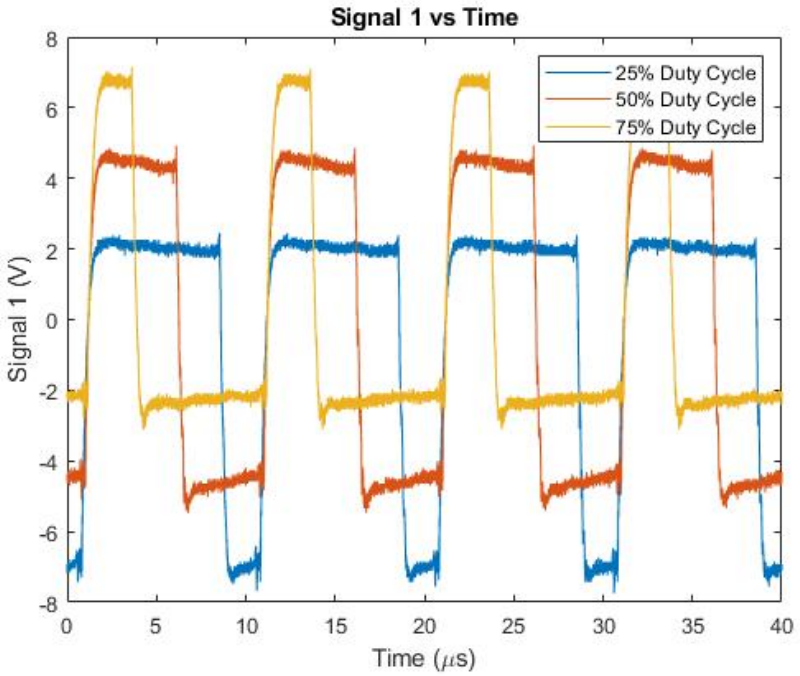


Figure 55: Amplitude scaling circuit Signal 1 output when Cs is 14 pF.

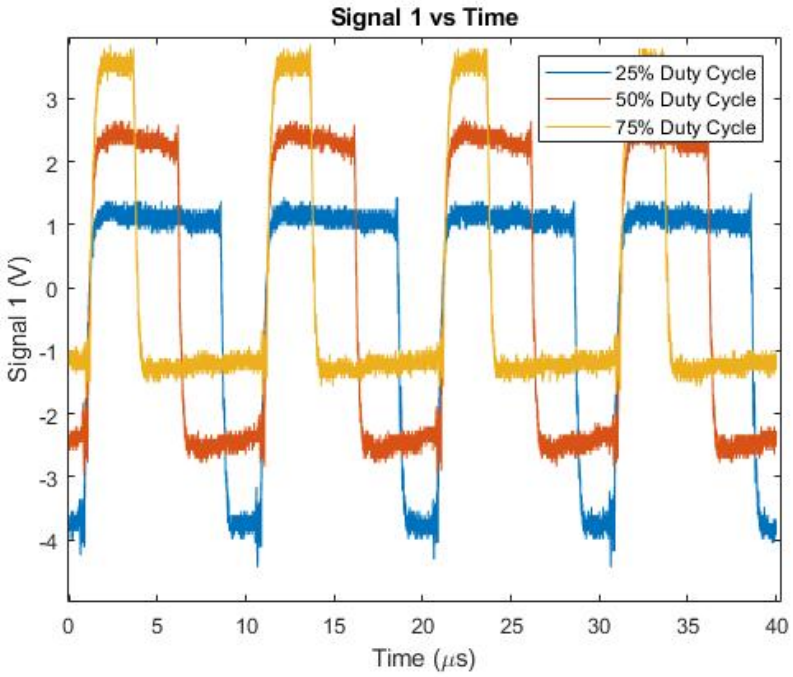


Figure 56: Amplitude circuit Signal 1 output when Cs is 7 pF.

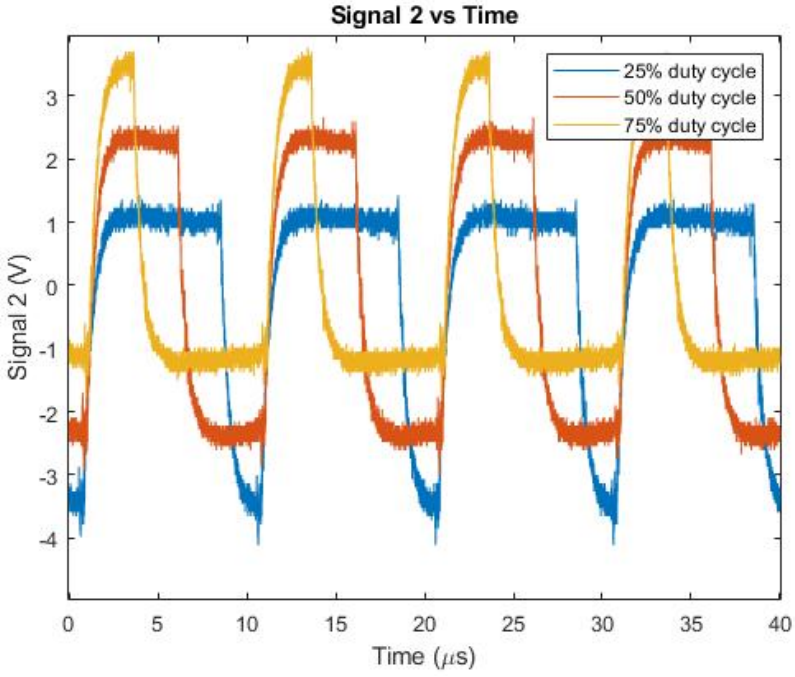


Figure 57: Signal 2 output.

Table 11: Amplitude scaling circuit capacitance estimate.

Cs (pF)	DC	$\mathbf{B_0}$	$\mathbf{B_1}$	$\overline{\textbf{Cest}}$ **(pF) (n = 20)**	**Std Dev (pF)**
14	75	1.1	2	16.233	.163
14	50	1.1	2	16.529	.283
14	25	1.1	2	16.659	.130
7	75	1.1	2	8.635	.796
7	50	1.1	2	8.697	.797
7	25	1.1	2	8.726	.104

4.4.2.2 Amplitude Integrating Circuit Analysis

Next, the high pass variant is read through the integrator circuit. The integrator circuit in the high pass variant case performs the same way as the integrator circuit in the all pass filter variant, except for one key difference. As the high pass filter stabilizes, over one period the area under the curves becomes zero. As a result, after one integration cycle, the net integration becomes zero. Also, the triangle shaped signals are produced with different slants depending on the duty cycle. As a result, it is only possible to have one integration period for the high pass filter variant.

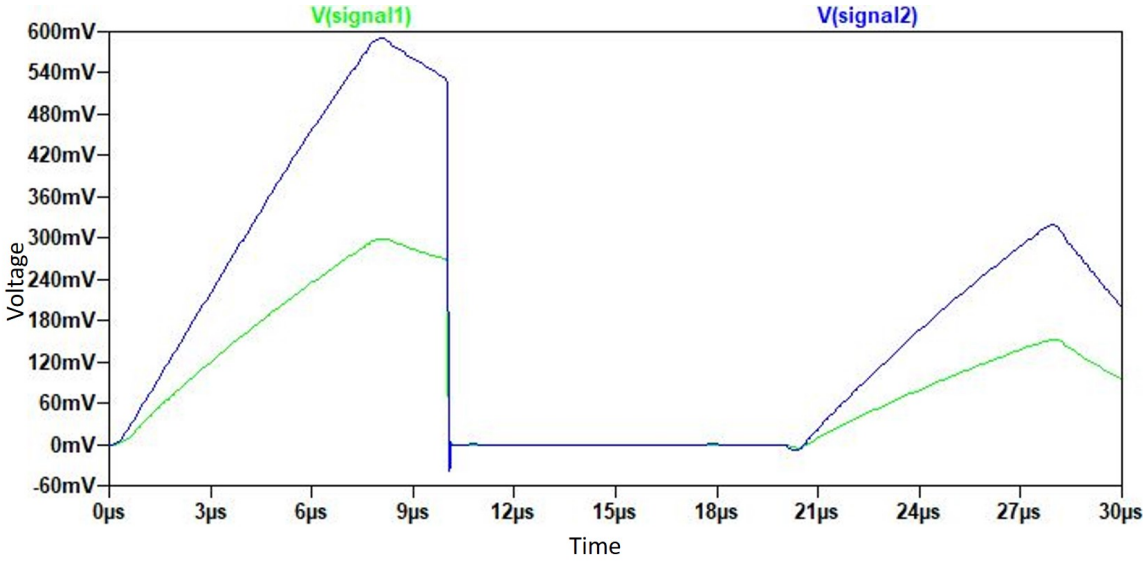


Figure 58: Signal 1 and Signal 2 simulation output for 1 integration periods.

Figure 58 shows the output obtained after running the LTspice® simulation on the integrator circuit. The first integration ends with a net increase because the circuit has not stabilized yet. However, as system stabilizes, the net energy integrated over time decreases to zero. When it comes to estimating the capacitance, the stabilization effect is not an issue because Signal 1 and Signal 2 stabilize at the same rate. In order to estimate the capacitance, voltage samples were taken at time 39.40678 microseconds. At this time, the voltage of Signal 1 equals 149.143 mV and the voltage of Signal 2 equals 300.78 mV. Using equations 8, 9, and 10 and the circuit gains (B_0=10, B_1 = 1), the estimated capacitance obtained is 10.43 pF. This is very close to the actual capacitance in the simulation of 10 pF. This difference can possibly be due to the nonideal circuit models, like the manufacturer opamp models, used. The simulation shows that this circuit can estimate the capacitance of the sense capacitor. The next step is to experimentally test the circuit.

The one integration period case was observed. The output voltages of Signal 1

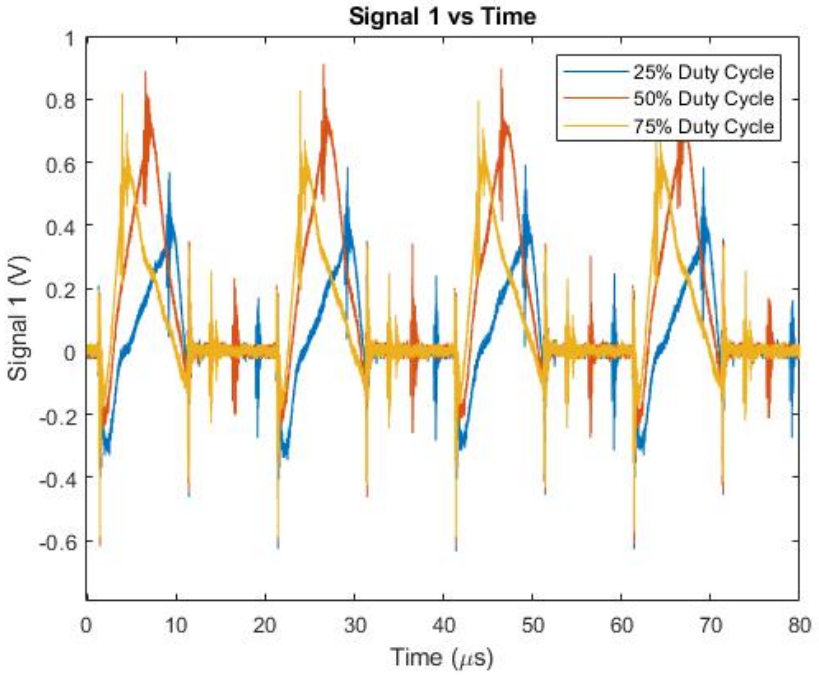


Figure 59: 1 integration period Signal 1 output when Cs is 14 pF.

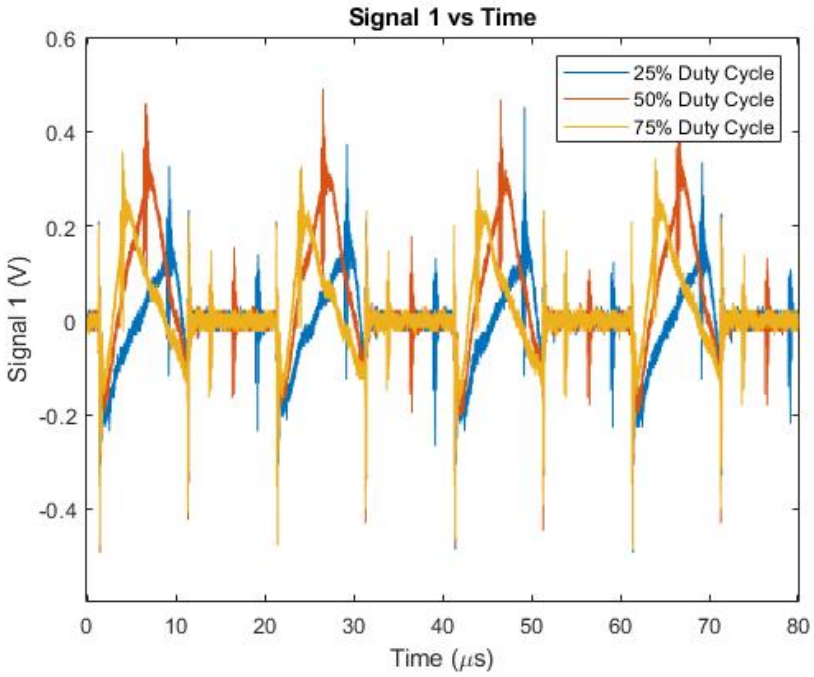


Figure 60: 1 integration period Signal 1 output when Cs is 7 pF.

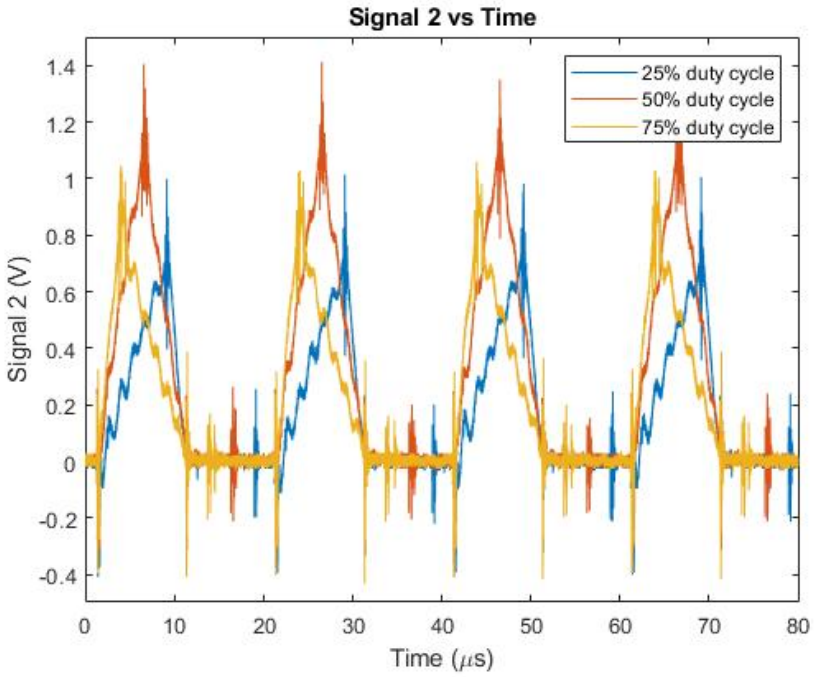


Figure 61: 1 integration period Signal 2 output is the same no matter what Cs.

when the sense capacitance is 7 picofarads and 14 picofarads and Signal 2 are shown in Figures 59, 60, and 61, respectively. The signals as a whole generate triangle waves however there are a couple of problems in the signals. First, the sides of the triangle waves are jagged lines, especially for Signal 2. This can be attributed to opamp overshoot instability that was not compensated. Another issue is Signal 1 has the same negative offset issue as the high pass filter except the offset is more severe (-.16 V). The next aspect to look at is the sense capacitance estimate.

From this data, the output voltages are sampled periodically over 200 microseconds and analyzed in MATLAB®. This gives 10 samples, which means the sampling period has doubled compared to the amplitude circuit. Table 12 shows the obtained capacitance estimate when the output data and the gain constants are plugged into equations 8, 9, and 10. The estimates of the sense capacitance in all cases are severely off although the difference in estimates is not as severe as before. When compensating

Table 12: 1 integration period capacitance estimate.

Cs (pF)	DC	$\mathbf{B_0}$	$\mathbf{B_1}$	$\overline{\textbf{Cest}}$ **(pF) (n = 10)**	**Std Dev (pF)**
14	75	10	1	10.097	.324
14	50	10	1	11.97	.173
14	25	10	1	11.699	.327
7	75	10	1	3.553	.295
7	50	10	1	4.634	.193
7	25	10	1	3.831	.315

Table 13: 1 integration period capacitance estimate compensated.

Cs (pF)	DC	**Comp.** $\overline{\textbf{Cest}}$ **(pF) (n = 10)**	**Comp. Std Dev (pF)**
14	75	15.493	.342
14	50	15.491	.169
14	25	16.476	.399
7	75	8.613	.308
7	50	7.923	.169
7	25	8.201	.296

for the -0.16 v input offset voltage, Table 13, the estimates of the sense capacitance are better. The estimates are closer to the sense capacitance and overestimate the sense capacitance.

Overall, the experimental outputs show that the amplitude scaling and amplitude integrating circuit work well with the high pass variant of the capacitor and are able to estimate and track the capacitance of the sense capacitor. Insofar the amplitude scaling circuit currently outperforms the amplitude integrating circuit in the high pass filter variant case in terms of noise, stability, and sampling rate.

V. Conclusions

This thesis analyzed the combination of using a PWM signal with a capacitor divider circuit for simultaneous control and actuation of electrostatic MEMS. This type of circuit has many benefits. First, simultaneous actuation and control allows for feedback control. Feedback control provides a system that is more controllable, more robust, and more stable. PWM drive circuits are cheaper then DC analog control circuits. Also, PWM circuits allow for one signal to both drive and sense an electrostatic MEMS. A capacitor divider has two distinct benefits: its simplicity to implement and high bandwidth [30]. A new variant, the high pass filter variant, was discussed and showed viability as an interface circuit for PWM actuation and sensing of electrostatic MEMS. This variant has the potential to perform better in terms of actuation than the traditional variant. Both variants, the all pass filter and high pass filter variants were analyzed using the amplitude scaling circuit and amplitude integrating circuits. The results show that the combination of a PWM driver circuit and a circuit divider interface circuit (in both high pass variant and low pass variant cases), are viable options for feedback control of electrostatic MEMS. The high pass filter variant is able to track the change in capacitance of the device as well as all pass filter variant. It is also a promising interface circuit for actuation of electrostatic MEMS. When designing the system the key design variables are summarized in the following list:

1. PWM Signal Characteristics: It is important to first select the PWM signals because they determine the design of the interface capacitance ratio, filters, and amplifiers/attenuators circuits.

    - Frequency: The frequency is lower bounded by the resonance frequency and upper bounded by the RC response time.

- Amplitude: The amplitude is chosen based on the actuation requirements of the system. The amplitude affects what kind of attenuation or amplification is needed in order to maximize the efficiency

2. Capacitor Divider Design Variables: This factor influences how drive signal is modulated into a sense signal that can be used to estimate the device capacitance.

    - Device Capacitance to Reference Capacitance Ratio: It is important to decide whether the capacitor will be in the top position or the bottom position of the capacitor divider circuit. This determines whether the voltage is high or low. It is also important to set the capacitance ratio less than 0.1 as to ensure that the input voltage is efficiently transferred across the actuator. The capacitance ratio also affects the sensitivity and resolution of the device.
    - Capacitor Divider Variants: High pass filter variant and all pass filter variant are two available design interface choices that produce different actuation signals across the device and different sense signals. These signals require different methods to extract the amplitude in order to estimate the capacitance.

3. Analog Signal Processing Scheme: This factor influences how the output signal from the interface signal is handled and what the signal to the ADC will look like. In this thesis, amplitude scaling and amplitude integration schemes were explored.

    - Amplitude Scaling: Advantage of the amplitude amplification circuit is that it requires the least amount of components and provides the quickest

response time. The disadvantage is that noise is amplified along with signal for V_{out} and the resolution is lower.

- Amplitude Integrating: The advantage of the the integrator circuit is that as the number of periods of integration increases, the resolution increases and the noise is averaged out. The disadvantage of this is that the response time increases.

5.1 Future Work

The following future work is recommended in order to create a simultaneous actuation and sensing circuit for an electrostatic MEMS.

- Analyze how electrostatic devices actuate when placed in the interface circuit of both capacitor divider variants. In the all pass variant case there is a golden ratio where you will get the best actuation per duty cycle. In the high pass filter case, the ratio may be different as dc bias offset that increases with duty cycle can improve the relationship between the force actuated and the duty cycle.

- Reduce noise and instability associated with the circuits in order to improve the efficiency, reliability, resolution, and accuracy of the system. This will allow for more confidence in the circuit in order to transition into feedback control.

- Perform feedback position control of an electostatic MEMS using the proposed circuits, an electrostatic MEMS, and a micro-controller. The micro-controller can replace the signal generators to control the MOSFET driver. It will also provide the ADC to receive the sensing signals to estimate the capacitance of the actuator. The signals received by the ADC can then be used to estimate the position of the actuator and provide feedback for the micro-controller.

By accomplishing these tasks a complete simultaneous actuation and sensing circuit can be created. This will lead to a number of benefits for the Air Force. First, this circuit can be used to actuate and sense many Air craft present or future systems like Chemical attack warning sensors, active surfaces, microrobotic electronic disabling systems, etc. [39] Second, this system uses a more inexpensive drive circuit than analog control systems. Third, a simultaneous actuation system will increase the performance and lifetime of MEMS devices. Lastly, with a more robust, accurate, and sensitive performance, the control circuit will be able to use MEMS devices for more complicated tasks that requires feedback control.

Appendix A. Additional Results

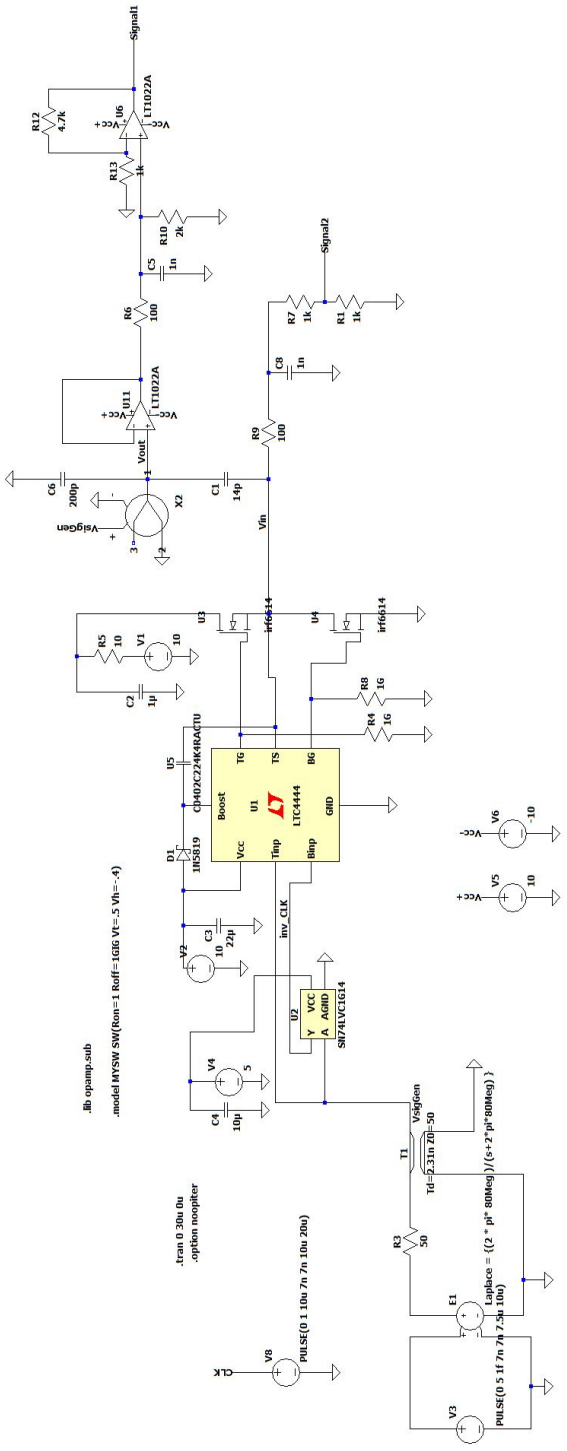


Figure 62: Complete All pass amplitude circuit schematic.

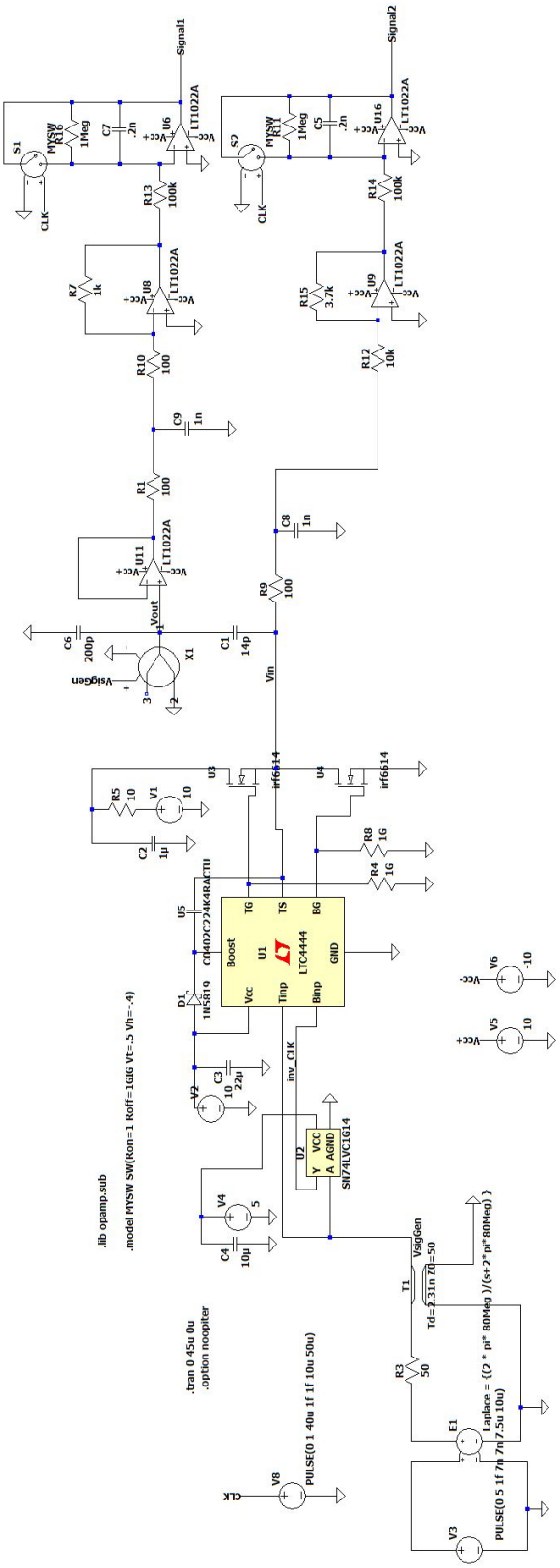


Figure 63: Complete all pass integrator circuit schematic.

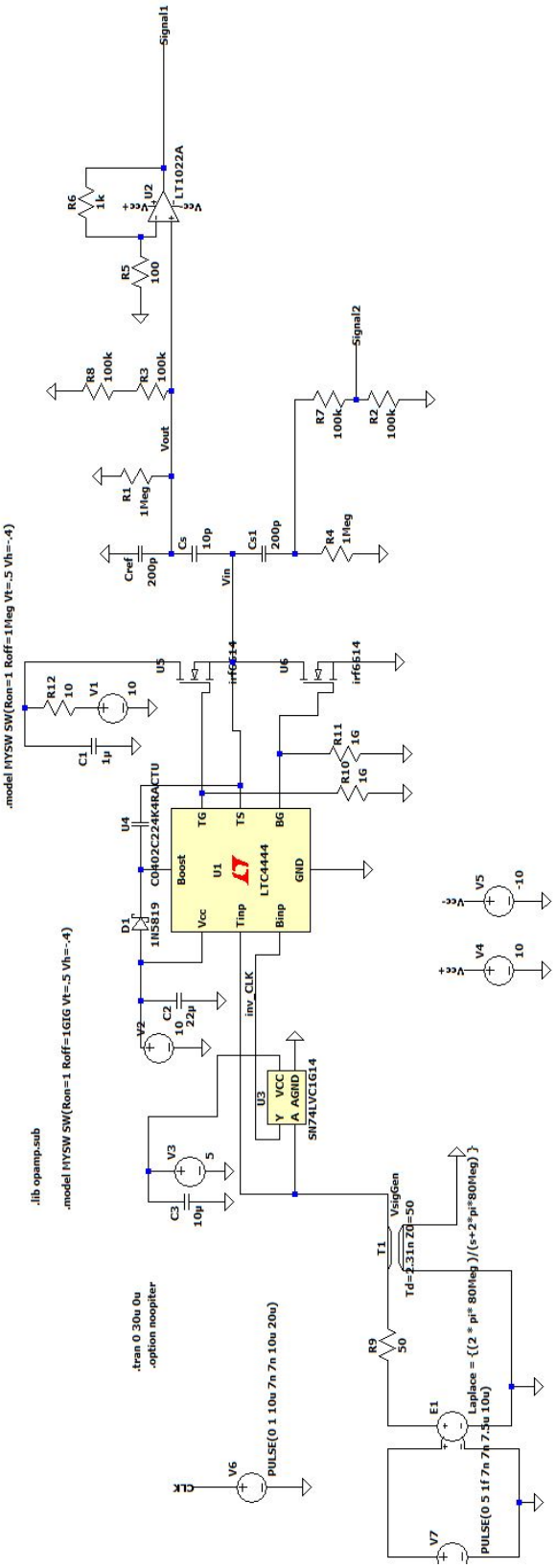


Figure 64: Complete high pass amplitude circuit schematic.

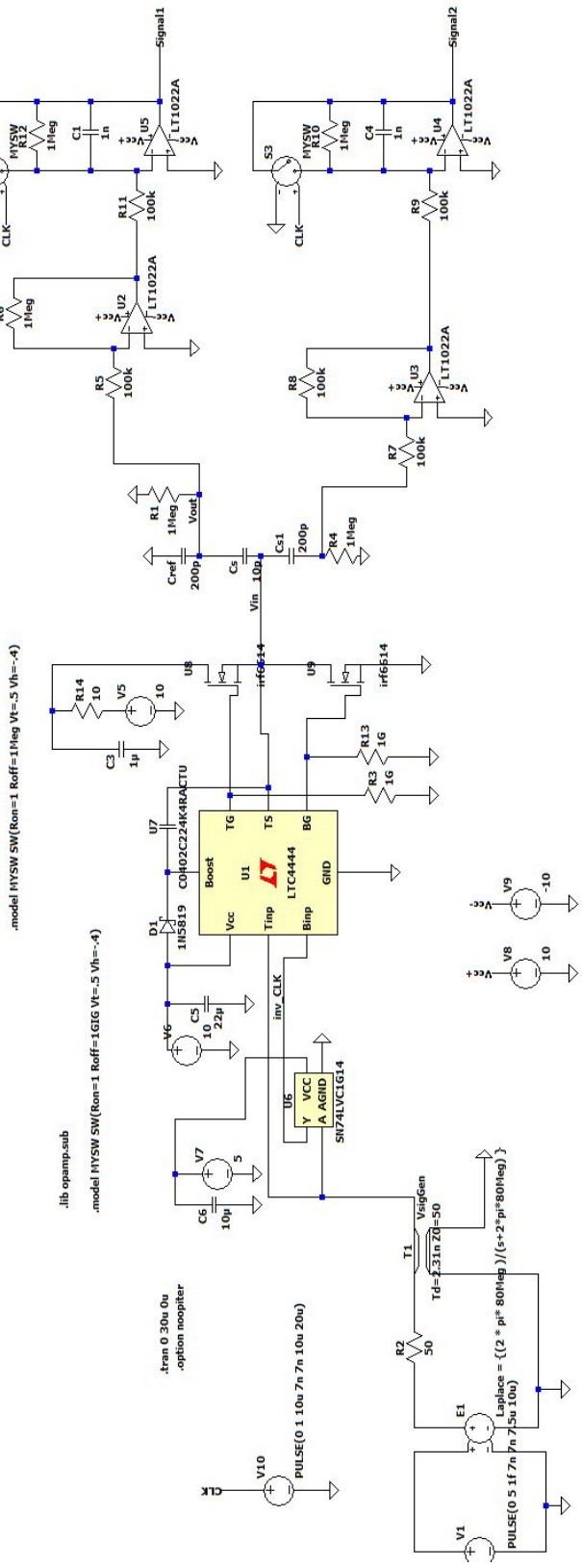


Figure 65: Complete high pass integrator circuit schematic.

Bibliography

1. Yole Developpement. Status of MEMS Industry 2021. Technical report, 2021.

2. C. Todd Lopez. DOD Adopts 'Zero Trust' Approach to Buying Microelectronics, 2020.

3. Manish Kumar Mishra, Vikas Dubey, P. M. Mishra, and Isharat Khan. MEMS Technology: A Review. *Journal of Engineering Research and Reports*, 4(1):1–24, 2019.

4. EEHerald. Introduction and application areas for MEMS, 2017.

5. Nadim Maluf and Kirt Williams. *An Introduction to Microelectromechanical Systems Engineering*. 2nd edition, 2014.

6. F. Chollet and HB LIU. A (not so) short introduction to MEMS, 2020.

7. Mohamed Gad-El-Hak. *MEMS: Introduction and fundamentals*. 2005.

8. SR Karumuri, Y Srinivas, JV Sekhar, and KG Sravani. Review on break through MEMS Technology. *Archives of Physics Research*, 2(4):158–165, 2011.

9. Henry H. Radamson, Jun Luo, Eddy Simoen, and Chao Zhao. *CMOS Past, Presemt, and Future*. 2018.

10. PRIME Faraday Partnership. *An Introduction to MEMS*. 2002.

11. MEMSCAP. The Power of a Small World.

12. David Lammers. Power Struggle — Applied Materials, 2013.

13. Applied Materials. Power Struggle.

14. Susumu Sugiyama. Progress of Integration in MEMS and New Industry Creation.

15. James J. Allen. Micro Electro Mechanical System Design. *Micro Electro Mechanical System Design*, 2005.

16. Abdullah Saleh Algamili, Mohd Haris Md Khir, John Ojur Dennis, Abdelaziz Yousif Ahmed, Sami Sultan Alabsi, Saeed Salem Ba Hashwan, and Mohammed M. Junaid. A Review of Actuation and Sensing Mechanisms in MEMS-Based Sensor Devices. *Nanoscale Research Letters*, 16(1), 2021.

17. Slava Krylov, Bojan R. Ilic, David Schreiber, Shimon Seretensky, and Harold Craighead. The pull-in behavior of electrostatically actuated bistable microstructures. *Journal of Micromechanics and Microengineering*, 18(5), 2008.

18. Mohammad Tausiff, Hassen M. Ouakad, Hussain Alqahtani, and Abdurahman Alofi. Local nonlinear dynamics of MEMS arches actuated by fringing-field electrostatic actuation. *Nonlinear Dynamics*, 95(4):2907–2921, 2019.

19. Jason M Edwards. Modeling and Feedback Control of a Mems Electrostatic Actuator. 2008.

20. Ki Bang Lee. *Principles of Microelectromechanical Systems*. 2011.

21. M Elwenspoek, Rob Legtenberg, and a W Groeneveld. Comb-drive actuators for large displacements. *Journal of Micromechanics and Microengineering*, 6(3):320–329, 1999.

22. Gülşah Demirhan. *RESONANCE-BASED MEMS TEMPERATURE SENSORS FOR TEMPERATURE COMPENSATION OF MEMS CAPACITIVE ACCELEROMETER*. PhD thesis, 2016.

23. V. P. Petkov and B. E. Boser. *Capacitive Interfaces for MEMS*, volume 1. 2004.

24. ViewSonic. What to Look for in a DLP Projector - ViewSonic Library.

25. Mark N. Horenstein, Julie A. Perreault, and Thomas G. Bifano. Differential capacitive position sensor for planar MEMS structures with vertical motion. *Sensors and Actuators, A: Physical*, 80(1):53–61, 2000.

26. Corey Pollock, Lawrence K. Barrett, Pablo G. Del Corro, Alexander Stange, Thomas G. Bifano, and David J. Bishop. PWM as a low cost method for the analog control of MEMS devices. *Journal of Microelectromechanical Systems*, 28(2):245–253, 2019.

27. Thorlabs. MEMS-Based Deformable Mirrors.

28. Javier Pérez Sanjurjo, Enrique Prefasi, Cesare Buffa, and Richard Gaggl. A Capacitance-To-Digital Converter for MEMS Sensors for Smart Applications. *Sensors (Basel, Switzerland)*, 17(6):1–17, 2017.

29. Robert Conant, C A Us, William Clark, and C A Us. PWM-based measurement interface for a micromachined electrostatic actuator, 2004.

30. Daniel Fernández, Jordi Madrenas, Manuel Domínguez, Joan Pons, and Jordi Ricart. Pulse drive and capacitance measurement circuit for MEMS electrostatic actuators. *Analog Integrated Circuits and Signal Processing*, 57(3):225–232, 2008.

31. Minhang Bao. Analysis and Design Principles of MEMS Devices. *Analysis and Design Principles of MEMS Devices*, 2005.

32. Richard Schroedter, Han Woong Yoo, David Brunner, and Georg Schitter. Capacitive Charge-based Self-Sensing for Resonant Electrostatic MEMS mirrors. *21th IFAC World Congress*, 2020.

33. Steven Ian Moore and S. O.Reza Moheimani. A switched actuation and sensing method for a MEMS electrostatic drive. *Proceedings of the American Control Conference*, 2016-July:5817–5822, 2016.

34. Fatemeh Aezinia. *Design of interface circuits for capacitive sensing applications*. PhD thesis, University of Tehran, 2014.

35. Navid Yazdi, Haluk Kulah, and Khalil Najafi. Precision readout circuits for capacitive microaccelerometers. *Proceedings of IEEE Sensors*, 1(2):28–31, 2004.

36. Chao Lin Cheng, Heng Chung Chang, Chun I. Chang, Weileun Fang, Munseon Jang, Kwang Seok Yun, Wen Chien Chen, Weileun Fang, Sheng Shian Li, Po Chun Chuang, Kuei Ann Wen, and Lasse Aaltonen. *Integrated Interface Electronics for Capacitive Mems Inertial Sensors*, volume 0. 2010.

37. Daniel Fernández, Jordi Madrenas, Manuel Domínguez, Joan Pons, and Jordi Ricart. PULSE-DRIVE AND CAPACITIVE MEASUREMENT CIRCUIT FOR MEMS ELECTROSTATIC ACTUATORS. (April):25–27, 2007.

38. S P Selvaraj, S Dhashnamoorthy, M Dhurun, and V Kishore. PLC Based Temperature Controlling using Peltier Element for Industrial Automation. pages 2242–2245, 2020.

39. Keith W. Brendley and Randall Steeb. Military Applications of Microelectromechanical Systems. Technical report, 1993.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704–0188

1. REPORT DATE *(DD–MM–YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From — To)*
24–03–2022	Master's Thesis	Sept 2020 — Mar 2022

4. TITLE AND SUBTITLE

Simultaneous Actuation and Sensing of Electrostatic MEMS

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

Jacob E. Song

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Air Force Institute of Technology
Graduate School of Engineering and Management (AFIT/EN)
2950 Hobson Way
WPAFB OH 45433-7765

8. PERFORMING ORGANIZATION REPORT NUMBER

AFIT-ENG-MS-22-M-063

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Intentionally Left Blank

10. SPONSOR/MONITOR'S ACRONYM(S)

Intentionally Left Blank

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

Intentionally Left Blank

12. DISTRIBUTION / AVAILABILITY STATEMENT

DISTRIBUTION STATEMENT A:
APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

Micro-Electro-Mechanical Systems (MEMS) are devices that play important roles of sensing and actuation in many different industries including automation, electronics, medical, communications, and defense. In order to make full use of these devices, it is important to understand the peripherals that enable these devices. Simultaneous actuation and control of MEMS is an important area of research as it enables feedback control of these devices and allow them to maintain performance as they depreciate over their lifetime. The aim of this thesis is to perform a design space analysis on an electrostatic MEMS simultaneous actuation and sensing circuit that is driven by a Pulse Width Modulated (PWM) signal and sensed by a capacitor divider interface circuit. A new variant to the capacitor divider interface is discussed and takes advantage of the leakage problem associated with this circuit. Furthermore, the important design variables and their impacts are investigated. The results found herein are generalized and may be applied to any electrostatic MEMS.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Capt Matthew J. Vincie, Ph.D, AFIT/ENG
U	U	U	UU	96	19b. TELEPHONE NUMBER *(include area code)* (937) 255-3636 x4711; Matthew.Vincie@afit.edu