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Bipolar Cascade Vertical Cavity Surface Emitting Lasers for RF Photonic Link Applications

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BIPOLAR CASCADE VERTICAL-CAVITY SURFACE-EMITTING LASERS FOR RF PHOTONIC LINK APPLICATIONS

DISSERTATION

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AFIT/DS/ENG/07-22

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Abstract

Large, phased-array apertures for aerospace reconnaissance will require radio-frequency (RF) photonic interconnects or links. Optical links will provide a host of essential functions such as true time delay and wideband local communication. Fiber-based links are low mass, easily reconfigurable, and relatively impervious to temperature. Unfortunately, the standard RF-optical-RF conversion introduces insertion losses of 20 dB or more.

There are four primary factors that cause large insertion losses in RF photonic links: (1) a large impedance mismatch; (2) the modulation efficiency of laser diodes is low; (3) the optical detectors have poor gain; and (4) not all of the light is coupled into and out of the optical fiber. To avoid the resulting packaging and parasitic issues, the development of monolithically-integrated semiconductor laser stacks was determined to be a promising candidate for a direct-drive RF photonic link device.

In this dissertation, the development and demonstration of bipolar cascade (BC) vertical cavity surface emitting lasers (VCSEL) is presented. The systematic approach to designing, fabricating, and characterizing the critical tunnel junction, incorporating the tunnel junction into an edge emitting bipolar cascade laser, and finally the transition to a VCSEL structure is detailed. A novel approach prior to growing and characterizing BC VCSELs was to investigate bipolar cascade light emitting diodes which incorporate the microcavity designs and disentangles the VCSEL cavity effects from the microcavity.

The best performing p-doped oxide aperture microcavity design was then used as the microcavity for 1-, 2-, and 3-stage BC VCSELs. The high-frequency modulation characteristics of GaAs-based BC VCSELs operating at 980 nm with GaAs tunnel junctions and p-doped $Al_{0.98}Ga_{0.02}As$ oxide apertures have been measured and analyzed. Measured -3 dB laser output modulations of 4.5 GHz for 2-stage and 7.1 GHz for 3-stage devices in response to small-signal current injection at an operating temperature of -50 °C are reported and discussed.

Acknowledgements

First and foremost I want to give all praise and glory to the Father, the Son, our Savior Jesus Christ, and the Holy Spirit. Their love and guidance has given me the strength to persevere in the toughest time in my life.

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William J. Siskaninetz

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V_0	Built-In Voltage	9
ϵ	Permittivity	9
E_{gap}	Bandgap Energy	9
$D(qV)$	Overlap Integral	9
J_{valley}	Current Density at Base of NDR	9
V_{valley}	Voltage at Base of NDR	9
n_i	Intrinsic Carrier Concentration	10
D_n	Electron Drift Diffusion coefficient	10
D_p	Hole Drift Diffusion Coefficient	10
τ_n	Electron Lifetime	10
τ_p	Hole Lifetime	10
AlAs	Aluminum Arsenide	12
InGaP	Indium gallium Phosphide	12
$\eta_{d-device}$	Device Differential Quantum Efficiency	13
h	Plank's Constant	13
c	Velocity of Light	13
Be	Beryllium	15
Sn	Tin	15
Ti	Titanium	15
Au	Gold	15
InGaAsP	Indium Gallium Arsenide Phosphide	15
S	Sulfur	15
C	Carbon	15
Pt	Platinum	16
H_3PO_4	Phosphoric Acid	16
H_2O_2	Hydrogen Peroxide	16
Zn	Zinc	16
Si	Silicon	16

Symbol		Page
Ge	Germanium	18
Ni	Nickel	18
AlInGaAs	Aluminum Indium Gallium Arsenide	19
x_w	Depletion Width	23
T	Temperature	23
$f_n(E)$	Electron Fermi Occupation Probability	24
$f_p(E)$	Hole Fermi Occupation Probability	24
$\rho_e(E)$	Electron Density of States	24
$\rho_h(E)$	Hole Density of States	24
E_c	Conduction Band Energy	24
E_v	Valence Band Energy	24
N_d^+	Ionized Donor Concentration	24
N_a^+	Ionized Acceptor Concentration	24
g_d	Donor Degeneracy	25
g_a	Acceptor Degeneracy	25
E_d	Donor Binding Energy	25
E_a	Acceptor Binding Energy	25
E_F	Fermi Energy	25
Ar	Argon	49
H_2	Hydrogen Gas	49
BCl_3	Boron Trichloride	49
Cl_2	Chlorine	49
MTF	Modulation Transfer Function	64
ω	Angular Frequency	64
$\omega_r = 2\pi f_r$	Relaxation Oscillation Frequency	64
γ	Damping Factor	64
C_m	Single Pole Amplitude MTF Constant	64
C_{par}	Parasitic Amplitude Constant	64

Symbol		Page
τ_{par}	Parasitic Time Constant	65
f_{par}	Parasitic Frequency	65
f_{peak}	Peak Frequency	65
$f_{-3\ dB\ Calc}$	Calculated -3 dB Frequency	65
η_{slope}	Slope Efficiency	67
I_{th}	Threshold Current	69
$\eta_{wallplug}$	Wall-plug Efficiency	69
$I_{freq\ resp}$	Frequency Response Drive Current	69
$f_{-3\ dB\ Meas}$	-3dB Frequency	69

List of Abbreviations

BIPOLAR CASCADE VERTICAL-CAVITY SURFACE-EMITTING LASERS FOR RF PHOTONIC LINK APPLICATIONS

I. Introduction

1.1 Problem

Large, phased-array apertures for aerospace reconnaissance will require radio frequency (RF) photonic interconnects or links. Optical links will provide a host of essential functions such as true time delay and wideband local communication. Fiber-based links are low mass, easily reconfigurable, and relatively impervious to temperature. The combination of increased functionality, reduced launch costs, and environmental insensitivity will allow RF photonic links to enable future generations of multimission surveillance satellites. Unfortunately, the standard RF-optical-RF conversion introduces insertion losses of 20 dB or more. In land-based telecommunication systems, these losses can be tolerated. In space systems, power is always at a premium, and RF signal power is the most precious of all. Therefore, space-based RF photonic link research is ongoing.

An RF photonic link consists of three primary components: (1) an RF-to-optical modulation component; (2) an optical-to-RF demodulation component; and (3) the transmission medium which can be a short ($<$ 1 km) optical fiber or free-space. The RF-to-optical modulation component can be either a direct-drive component where a semiconductor laser is directly driven by current modulating the RF signal or externally driven where a CW laser is combined with the RF source in an external modulator.

There are four primary factors that cause large insertion losses in RF photonic links: (1) a large impedance mismatch between conventional laser diodes and standard RF microelectronics causes most of the RF power transmitted to the laser diode to be reflected;

(2) the modulation efficiency of the laser diodes is somewhat low, so strong electronic RF waveforms become comparatively weak optical waveforms; (3) the optical detectors have poor gain and are not impedance matched to the antenna; and (4) not all of the light is coupled into and out of the optical fiber or detection system.

Of these factors, (1) and (2) are by far the most important. They can both be mitigated by stacking N (an integer) semiconductor lasers in series. By choosing N properly, the stack impedance can match the RF driving circuit to solve problem (1). This approach addresses problem (2), as well, since it also increases the optical output power and modulation efficiency by up to a factor of N. On paper, a series laser stack looks like an ideal solution, and can even provide RF gain as opposed to loss. But, there are two serious drawbacks to this straightforward approach: (1) the resulting packaging costs are very high, and a fully-interconnected phased-array of such sources is prohibitively expensive; and (2) the multitude of solder bonds between devices induce large parasitics and dramatically increases the sensitivity to thermo-mechanical stress. Therefore, such series laser stacks will perform sub-optimally and exhibit low reliability.

1.2 Objective

To avoid the resulting packaging and parasitic issues, the development of monolithically integrated semiconductor laser stacks was determined to be a promising candidate for a direct-drive RF photonic link device. This bipolar cascade (BC) laser consists of more than one multiple quantum well (QW) active region (AR) separated by at least one reverse biased tunnel junction (TJ). To achieve single mode output, a vertical-cavity surface emitting laser (VCSEL) is required to allow for the increased number of ARs, TJs, and oxide apertures (OA) in an $\frac{n}{2}\lambda$ optical cavity, where n is a positive integer. The design, growth, fabrication, and characterization of BC VCSELs operating primarily at 980 nm was performed at the Air Force Research Laboratory. The laser development was accomplished using the GaAs/AlGaAs/InGaAs material system, rather than the InP-based material system because (1) the higher bandgap of GaAs relative to InP gives better temperature performance, and (2) the index contrast between GaAs and high Al content AlGaAs is much

greater than the index contrast in AlInP resulting in fewer distributed Bragg reflector (DBR) mirror pairs during laser growth. $In_{0.2}Ga_{0.8}As$ quantum wells, operating at 980 nm, were chosen because strained InGaAs quantum wells exhibit superior high-speed performance. Telecommunication wavelengths of 1.3 μm and 1.55 μm are the "holy grail" for bipolar cascade lasers. However, any direct-drive RF photonic link application will essentially be a local area network and loss due to attenuation will be relatively negligible in short ($<$1 km) lengths of optical fiber. Attenuation in a single-mode silica fiber at 1.55 μm is 0.15 dB/km, at 1.3 μm is 0.30 dB/km, and at 980 nm is only 0.90 dB/km [31]. The direct-drive methodology also releases the system designer from the telecommunication requirements because the externally driven modulation system is required to operate with telecommunication lasers, whereas the direct-drive approach combines the laser and modulation.

The research plan approved by the dissertation committee after the prospectus defense was to systematically develop room-temperature operating BC VCSELs for RF photonic link applications. The quantifiable goals are to demonstrate room-temperature high-speed BC VCSELs with (1) device slope efficiencies greater than 1 W/A, (2) small-signal modulation $>$5 GHz, and (3) improved impedance matching.

1.3 Approach

To develop BC VCSELs, several systematic steps were required. First and foremost was to develop a robust GaAs-based tunnel junction layer structure. This required verifying carbon-doped GaAs limitations, developing and verifying silicon δ-doped GaAs layer structure limitations, and combining the two layers to develop GaAs:C / GaAs:Si tunnel junctions.

The next systematic step was to develop an edge-emitting gain-guided bipolar cascade laser (BCL). This was done in multiple stages to verify the series connected lasers were operating as expected. The first stage was to design and demonstrate multi-color multiple-cavity BCLs to verify multiple laser operation. This allowed for spectral verification along with current versus voltage verification of BCL operation. The second stage was to design and demonstrate single-color multiple-cavity BCLs to verify improved device

differential quantum efficiency (demonstrated differential quantum efficiencies greater than 1). The final stage was to design and demonstrate single-color single-cavity BCLs and verify single-cavity single-longitudinal mode laser operation. This last stage verified that the cavity thickness for single spatial mode edge-emitting lasers is too small to accommodate tunnel junctions and active regions.

The next systematic step was to develop BC VCSELs. This was also accomplished in multiple stages. The first stage was to design the BC VCSEL in a modular fashion so additional stages and reordering the active region, tunnel junction and oxide aperture could be quickly modeled and studied. The second stage was to disentangle the physics of the microcavity from the VCSEL cavity and study the microcavity designs in a BC LED structure. This allowed for rapid growth, fabrication and characterization of numerous designs studying oxide aperture doping type and arrangement of microcavity structures. Finally, the best performing BC LED microcavity design was incorporated into a VCSEL structure and 1-, 2-, and 3-stage BC VCSELs were grown, fabricated, and characterized for laser and high-speed operation.

1.4 Summary of Significant Results

The high-frequency modulation characteristics of GaAs-based bipolar cascade vertical cavity surface-emitting lasers operating at 980 nm with GaAs tunnel junctions and p-doped $Al_{0.98}Ga_{0.02}As$ oxide apertures have been measured and analyzed. Slope efficiencies of 0.46 W/A and 0.36 W/A and -3 dB modulation bandwidths of 7.1 GHz and 4.5 GHz were measured for the 3- and 2-stage devices, respectively, at an operating temperature of -50 °C for devices with 28 μm diameter mesas corresponding to 8 μm oxide aperture. The 3-stage device operated at room temperature with a slope efficiency of 0.1 W/A and a -3 dB modulation bandwidth of 3.2 GHz.

This research represents the first demonstration of frequency response in BC VCSELs. While this research did not achieve the desired 1 W/A goal it is still on par with the state-of-the-art (SOA). The combination of large slope efficiency and high-speed frequency modulation is a significant demonstration.

1.5 Document Organization

The outline of this document is much in line with the systematic approach laid out in Section 1.3. First it details the development of TJs both theoretically, experimentally, and by application. Second, the historical development of BCLs is presented. Third, the systematic development leading to the author's demonstration of BC VCSELs is presented. This systematic development details the GaAs-based TJ development, followed by edge emitting BCL advances, the BC LED investigation, followed by the BC VCSEL development an demonstration. Finally, the conclusions are presented including a summary of results and possibilities for future investigation.

II. Background

2.1 Degenerate Tunnel Junctions

Semiconductor tunnel junctions have been successfully designed and used in highly efficient solar cells [1]. For GaAs applications, δ-doping has been used to increase the effective doping concentration [9]. TJs are under investigation for integration into semiconductor laser devices (1) to improve laser slope efficiencies [18], (2) for impedance matching, (3) for multi-wavelength laser operation [12], (4) for high-power laser operation [24], (5) for reducing optical and free-carrier absorption [4], and (6) for use as current confinement apertures [33, 34]. This section describes the history of tunnel junction development, fundamentals of semiconductor tunnel junctions, and tunnel junction applications.

2.1.1 History. Tunnel junctions, also known as Esaki junctions, were discovered by L. Esaki at Bell Labs in 1958 [10]. Esaki was studying internal field emissions in a degenerately-doped germanium p-n junction when he noticed an "anomalous" current-voltage characteristic in the forward-biased direction. This "anomaly" was in the form of a negative differential resistance (NDR) region, which is the tell-tale signature of a good quality tunnel junction. Esaki was the first to describe this effect using the quantum tunneling concept and achieved reasonable results between tunneling theory and experimental results.

Further developments in tunneling theory and experimental techniques quickly followed. In 1961, Kane formulated a more complete theory of tunneling and developed the theoretical formulation for the peak current density required to calculate band-to-band tunneling [16]. Chynoweth $etal.$ soon followed also in 1961 with the formulation of the excess current component in tunneling devices [6]. Experimental validation of Esaki, Kane, and Chynoweth's predictions was accomplished by Meyerhofer $etal.$ in 1962 [27]. Demassa and Knott formulated a combined theory of Esaki and Kane's work for predicting tunnel junction behavior prior to device growth [8]. Roy further enhanced Demassa and Knott's work by including Chynoweth $etal.$ excess current component [30].

2.1.2 Fundamentals of Tunnel Junctions. A tunnel junction is a p-n junction where the p- and n-doped layers are degenerately doped [42]. Because of the high doping levels, the quasi-Fermi levels are located within the allowed bands. For tunneling to occur, four conditions must be achieved: (1) occupied energy states must exist from which the electrons are tunneling; (2) unoccupied energy states at the same energy levels to which the electrons are tunneling must exist; (3) a low potential barrier height must exist and a small barrier width are required for a non-zero tunneling probability; and (4) momentum must be conserved.

The current versus voltage (IV) characteristics for a tunnel diode, as shown in Fig. 2.1, is a summation of three current components

$$J = J_{tunnel} + J_{excess} + J_{thermal}. \tag{2.1}$$

These components are J_{tunnel}, the band-to-band tunneling current density, J_{excess}, the excess current density, and $J_{thermal}$, the minority-carrier diffusion current or thermal current density.

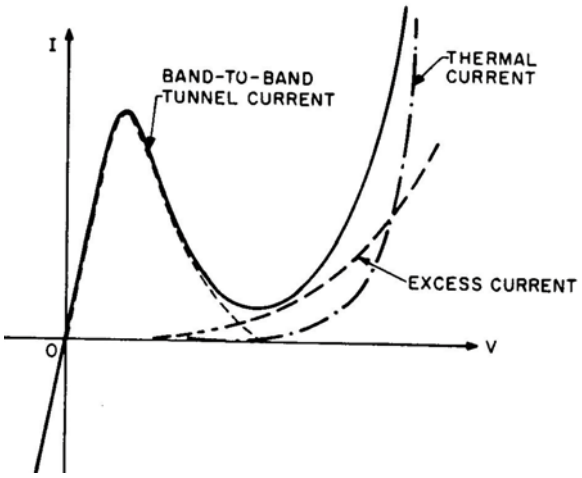


Figure 2.1: Diagram of a tunnel junction's IV characteristics illustrating the three current components [42].

The band-to-band tunneling current component is

$$J_{tunnel} = J_{peak} \left(\frac{V}{V_{peak}} \right) exp \left(1 - \frac{V}{V_{peak}} \right) \tag{2.2}$$

where V is the drive voltage, J_{peak} is the current density, and V_{peak} is the voltage at the onset of the negative differential resistance region, respectively. The term V_{peak} has been determined to be [16]

$$V_{peak} = \frac{V_n + V_p}{3} \approx \frac{k_B T}{3q} \left[\ln \frac{N_d}{N_c} + \ln \frac{N_a}{N_v} + 0.35 \left(\frac{N_d}{N_c} + \frac{N_a}{N_v} \right) \right] \tag{2.3}$$

where V_n is the amount of degeneracy on the n side [$V_n \equiv (E_{F_n} - E_C)/q$], where E_{F_n} is the electron quasi-Fermi energy and E_C is the conduction band energy. V_p is the amount of degeneracy on the p side [$V_p \equiv (E_V - E_{F_p})/q$], where E_{F_p} is the hole quasi-Fermi energy and E_V is the valence band energy. k_B is Boltzmann's constant, T is the temperature, q is the charge, N_d is the donor concentration, N_a is the acceptor concentration, N_c is the effective density of states in the conduction band defined as

$$N_c = 2 \left(\frac{m_e^* k_B T}{2\pi\hbar^2} \right)^{3/2} \tag{2.4}$$

where m_e^* is the electron effective mass and $\hbar$ is the reduced Plank's constant, and N_v is the effective density of states in the valence band defined as

$$N_v = 2 \left(\frac{(m_{hh}^* + m_{lh}^*) k_B T}{2\pi\hbar^2} \right)^{3/2} \tag{2.5}$$

where m_{hh}^* is the heavy hole effective mass and m_{lh}^* is the light hole effective mass.

J_{peak} has been determined to be

$$J_{peak} = \frac{1}{36\pi\hbar^2} \sqrt{\frac{q^5 m_{eff}^* N_{eff}^* V_o}{\epsilon E_{gap}}} \exp \left[\frac{-\pi}{2\hbar} \sqrt{\frac{\epsilon E_{gap}^3 m_{eff}^*}{q^3 N_{eff}^* V_o}} \right] D(qV) \tag{2.6}$$

where m_{eff}^* is the reduced effective mass defined as

$$m^*_{eff} = \frac{m^*_e(m^*_{hh} + m^*_{lh})}{m^*_e + (m^*_{hh} + m^*_{lh})} \tag{2.7}$$

N^*_{eff} is the reduced effective concentration defined as

$$N^*_{eff} = \frac{N_d N_a}{N_d + N_a} \tag{2.8}$$

V_0 is the built-in voltage, ϵ is the permittivity, E_{gap} is the bandgap energy and $D(qV)$ is the overlap integral.

The excess current component is

$$J_{excess} = J_{valley} \exp\left[\frac{4}{3}\left(\frac{m^*_{eff}\epsilon_s}{N^*_{eff}}\right)^{1/2}(V - V_{valley})\right] \tag{2.9}$$

where J_{valley} is the current density and V_{valley} is the voltage at the end of the negative differential resistance region. The excess current component is the most difficult term to determine theoretically because a high degree of knowledge of the growth conditions and environment must be known and quantified, so effects, such as from traps and dislocations, are known prior to device growth. Figure 2.2 illustrates a few ways excess current can occur in a structure. The pathways CAD and CBD occur due to deep level traps within the structure. The stair step example from C to D occurs due to local level transitions combined with a series of vertical steps in which the electron loses energy by transferring from one level to another. The final example, CABD, results in the electron dissipating its energy via impurity band conduction.

The final component, the thermal current (more commonly known as the minority carrier diffusion current) is

$$J_{thermal} = J_o\left[\exp\left(\frac{qV}{k_B T}\right) - 1\right] \tag{2.10}$$

where

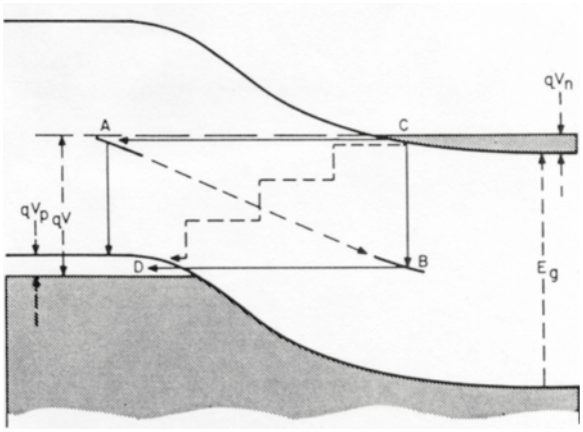


Figure 2.2: Example of a few tunneling pathways creating excess current [42].

$$J_o = qn_i^2 \left[\frac{1}{N_a}\sqrt{\frac{D_n}{\tau_n}} + \frac{1}{N_d}\sqrt{\frac{D_p}{\tau_p}} \right] \tag{2.11}$$

where n_i is the intrinsic carrier concentration, D_n is the electron drift diffusion coefficient, D_p is the hole drift diffusion coefficient, τ_n is the electron lifetime, and τ_p is the hole lifetime.

Qualitative descriptions of the band diagram and IV characteristics in various states of operation of a tunnel junction are shown in Figure 2.3. Figure 2.3 a) illustrates the reverse-biased configuration. Tunneling always occurs and the larger the reverse bias the larger the tunneling current. Figure 2.3 b) illustrates the device in thermal equilibrium. There is one Fermi energy level and no net current is generated. Figure 2.3 c) shows the effect of band-to-band tunneling. As the forward bias is increased, more occupied states on the electron side coincide with unoccupied states on the hole side. This occurs up to a maximum tunneling current where $E_{F_n} - E_V = E_C - E_{F_n}$ as shown in Figure 2.3 d). Figure 2.3 e) illustrates the NDR region where the overlap of occupied states on the electron side and the unoccupied states on the hole side decreases to a point where there is no longer any overlap between the two. The current does not go to zero because the excess current component is non-negligible. Finally, Figure 2.3 f) is the usual minority-carrier injection current or thermal current as obtained in standard p-n junction diodes.

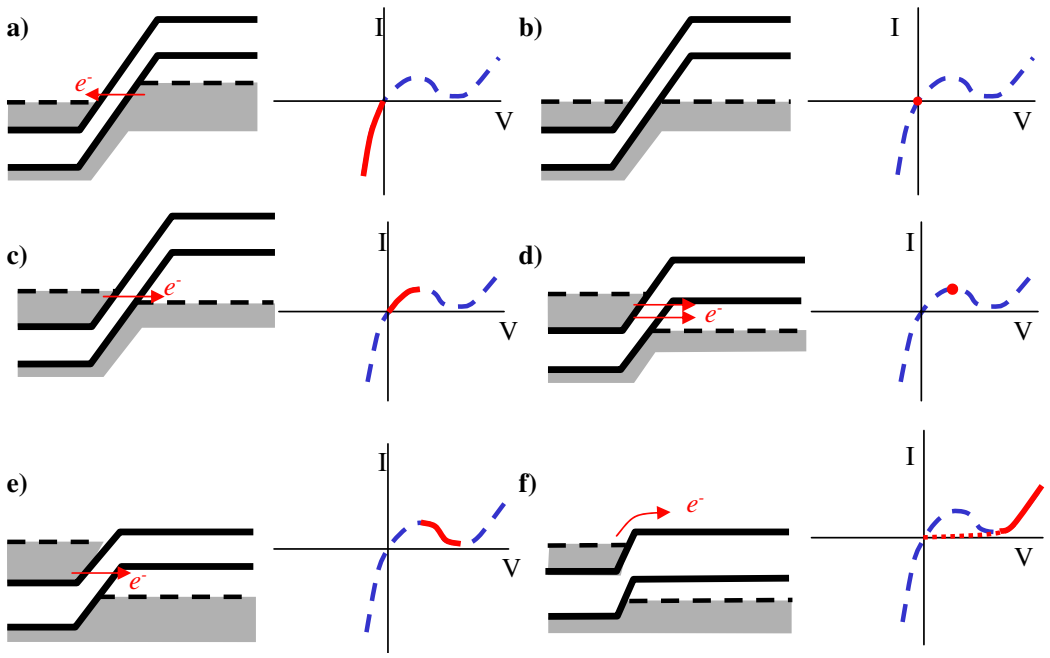


Figure 2.3: Qualitative description for a tunnel junction: a) reverse-biased tunneling, b) thermal equilibrium, c) forward-biased tunneling, d) maximum forward-biased tunneling current, e) negative differential resistance, f) minority-carrier injection current.

2.1.3 Tunnel Junction Applications. Tunnel devices were immediately recognized as candidates for microwave applications because the tunneling time of carriers through the potential energy barrier is not governed by the conventional transit time, but rather by the quantum transit probability per unit time which is much faster than the drift of minority carriers in standard p-n diodes. Tunnel junctions eventually gave way to faster electronic devices and are now rarely used for microwave applications. The next major application for tunnel junctions was in the development of tandem solar cells. This required significant research because these tunnel junctions were monolithically integrated during growth as a low-resistance interconnect between two different solar cells. This research is still ongoing and tandem solar cells are commercially available. Lately, tunnel junction research for other optoelectronic applications, primarily semiconductor lasers, has developed rapidly. Tunnel junctions are being developed as a means of monolithically connecting in series a number of different lasers, as electron-to-hole converters eliminating p-doped DBR mirrors in a VCSEL and as automatically formed tunnel apertures.

Research into low-resistance interconnects to monolithically integrate two different bandgap solar cells, known as tandem solar cells, has been ongoing since the late 1980s. Figure 2.4 is an illustration of some typical tandem solar cell designs. While this design is a GaAs/AlGaAs tandem solar cell, the highest efficiency solar cells are GaAs/InGaP devices with an efficiency $> 30\%$. Requirements include transparency to the lower solar cell, lattice matching to the substrate, and I_{peak} capable of carrying maximum photocurrent. Numerous material parameters have been studied. Growth parameters for molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), chemical beam epitaxy (CBE), and liquid phase epitaxy (LPE) have been developed and are still being refined. Doping materials and techniques to achieve degeneracy in these devices have been researched intensively. For GaAs-based structures, lattice-matched tunnel junctions made by GaAs, AlAs, AlGaAs, InGaP, and double heterostructure tunnel junctions have produced the most promise, depending on the application.

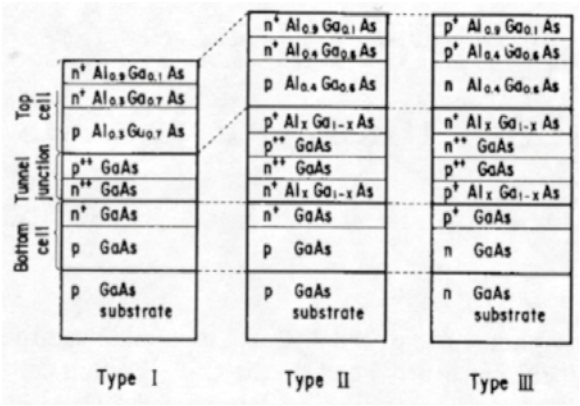


Figure 2.4: Schematic diagrams of some typical tandem solar cell designs [1].

2.2 Bipolar Cascade Lasers

2.2.1 Description. A BCL is an epitaxially-stacked number of semiconductor lasers separated by reverse-biased tunnel junctions, in which, valence-band electrons are "recycled" as conduction-band electrons. Edge-emitting lasers and VCSELs have been studied extensively over the past several decades and several textbooks have been written discussing the theory [5, 25, 29] and development [2, 7, 31, 46] of semiconductor lasers.

Typical semiconductor lasers are bipolar devices, because they are *p-i-n* devices. The reverse-biased TJ allows for the cascading of lasers by providing a low-resistance series interconnect between lasers. Ideally, if no scattering occurred at the tunnel junction and every electron injected recombined with a hole, the differential quantum efficiency for the entire device, $\eta_{d-device}$, would be equal to the differential quantum efficiency times the number of active regions cascaded. However, in reality, the differential quantum efficiency is defined as

$$\eta_d = 2\frac{\Delta L}{\Delta I}\left[\frac{q\lambda}{hc}\right] \tag{2.12}$$

where the 2 takes into account lasing from both facets, $\Delta L/\Delta I$ is the measured slope efficiency obtained from a light output power versus injected current (LI) curve, q is the electron charge, λ is the lasing wavelength, h is Planck's constant, and c is the speed of light. Since each active region has a differential quantum efficiency less than unity and there is scattering at the tunnel junction, the entire device quantum efficiency can be shown to be

$$\eta_{d-device} = \eta_d\left(N - M\delta N\right) \tag{2.13}$$

where N is the number of active regions, M is the number of tunnel junctions, and δN is the tunnel junction scattering efficiency. It is easily seen that the differential quantum efficiency for the entire device can be greater than unity with a simple example. Consider a device with two active regions separated by one tunnel junction and assume an $\eta_d \sim 0.6$ and scattering efficiency to be very small $\delta N \sim 0.05$. This yields an $\eta_{d-device}$ of 1.17.

However, this increase in efficiency does come at a cost. Effectively, each laser is connected in series; this means the voltage drop across the entire device increases linearly with the number of active regions incorporated into the device. The wall-plug power requirements still increase with increasing number of active regions. This will most likely result in a limit of how many lasers can be epitaxially cascaded.

Two different approaches to BCL growth can be taken. The first is to separate entire laser structures including the optical cladding by tunnel junctions. This is called a $multiple\ cavity$ or $intercavity$ device, as shown in Figure 2.5. The second approach incorporates all of the active regions within one optical cavity and separates the active regions by tunnel junctions. This is called an $intracavity$ device. This method is convenient for incorporating one or more tunnel junctions with a VCSEL structure, as well as engineering the cavity thickness so the tunnel junctions will reside in the optical mode nodes and the active regions will be in the optical mode antinodes.

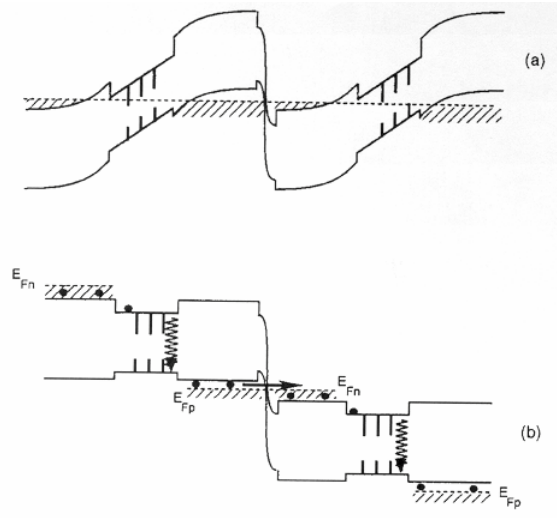


Figure 2.5: Schematic energy-band diagram of the epitaxially stacked laser at 0 V (a) and under forward-bias (b) [12].

2.2.2 Device History. The first demonstration of a BCL separated by a tunnel junction was in 1982 at Bell Laboratories [47]. However, further development languished until 1997 when researchers at Thomson CSF demonstrated a two-color BCL [12]. Since 1997, several research groups have begun studying BCLs using various material systems, in both edge emitting lasers and VCSELs, and for several specific applications.

2.2.3 Bell Laboratories. Researchers at Bell Labs first demonstrated a BCL by epitaxially layering three double-heterostructure GaAs lasers separated by highly-doped, reverse-biased tunnel junctions. On the left side of Figure 2.6 is a schematic of the epitaxial

layer structure. The laser sections consisted of 0.1 - 0.15 μm thick GaAs active regions and 1 - 2 μm thick p- and n-doped $Al_{0.3}Ga_{0.7}As$ cladding layers. The tunnel junctions were highly doped GaAs p^+n^+ layers ($\sim 10^{19}$ cm^{-3} Be for p and Sn for n) each $\sim$70 nm thick. The wafer was thinned to 100 μm and the p-ohmic was a Ti:Au alloy and the n-ohmic was a Sn-Au alloy. The width of the lasers was 100 μm and the cleaved lengths were 380 μm. The right side of Figure 2.6 shows the LI characteristics. The threshold current is $\sim$580 mA which yields a threshold current density of $\sim$1.4 kA/cm^2. The external differential quantum efficiency, η_d, is $\sim$0.8. The current measurements were performed using 200 ns pulses at a repetition rate of 1 kHz.

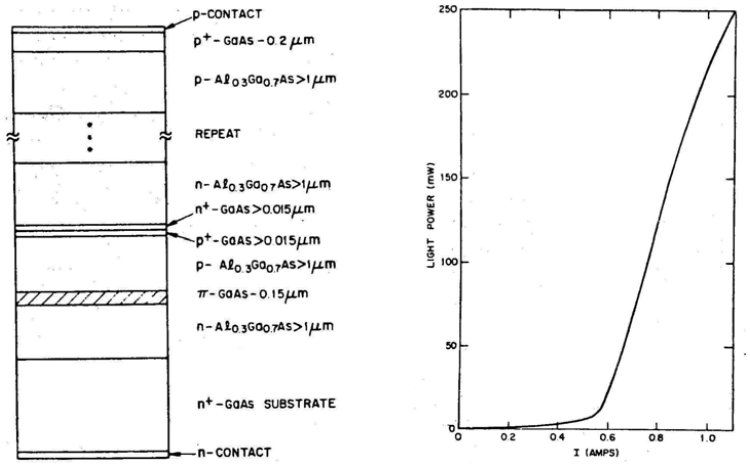


Figure 2.6: On the left is a schematic diagram of first successful BCL. The LI characteristics for Bell Labs three-layer laser obtained using 200 ns pulses at 1 kHz and at 300 K is shown on the right [47].

2.2.4 Thomson CSF. Researchers at Thomson CSF in France are investigating BCLs for high-power and multi-wavelength operation. They have reported the development of two different devices. The first is a two-color GaAs-based intercavity device with InGaAs QWs having operating wavelengths of $\sim$960 nm and $\sim$990 nm [12]. The second structure is a two-color InP-based intercavity device with InGaAsP QWs having operating wavelengths of $\sim$1520 nm and $\sim$1530 nm [24].

The GaAs-based intercavity laser structure, shown in Figure 2.7, was grown by CBE. The device consists of 1.5 μm thick S- and C-doped $Al_{0.45}Ga_{0.55}As$ cladding lay-

ers, and 1000 Å thick GaAs photon confinement layers. The top laser has three 80 Å thick $In_{0.12}Ga_{0.88}As$ QWs separated by 100 Å GaAs barriers. The bottom laser has three 80 Å thick $In_{0.15}Ga_{0.85}As$ QWs separated by 100 Å thick GaAs barriers. The tunnel junction consists of two 500 Å thick S-doped, 1.5×10^{19} cm^{-3}, and C-doped, 1×10^{20} cm^{-3}, layers. Gain-guided lasers were fabricated with the p-ohmic being a Ti:Pt:Au alloy and mesa etched by wet chemical etching (H_3PO_4:H_2O_2:H_2O) using the p-ohmic metal as the etch mask to a depth of 5 μm. The mesa etch helped to eliminate current spreading. The wafer was thinned and an n-ohmic metal was evaporated and the lasers were cleaved. Pulsed LI and spectral characterization was performed with a pulse width of 100 ns and a pulse repetition rate of 1 kHz on 850 μm long by 80 μm wide lasers. Figure 2.7 also shows the light versus current density and spectral characteristics. Two distinct threshold currents are evident, which is indicative of intercavity BCLs.

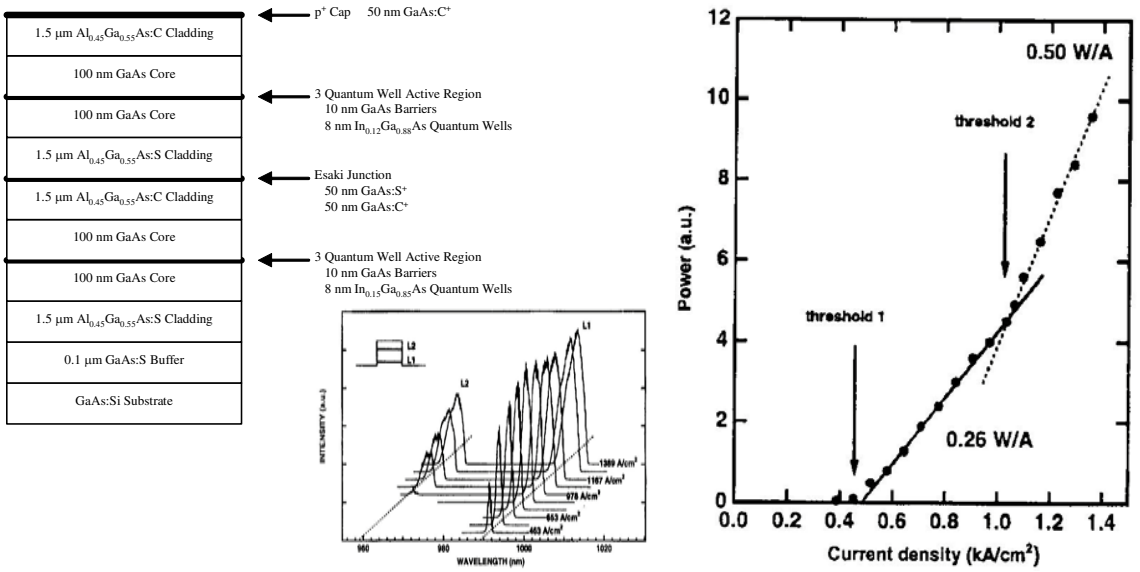


Figure 2.7: On the left is the schematic of the Thomson CSF layer structure of a 2-stage intercavity BCL. Light vs. current density (right) and spectral intensity as a function of current density (middle) for an 850 μm long and 80 μm wide InGaAs intercavity BCL [12].

The InP-based intercavity laser structure was grown by MOCVD. The device consists of 0.5 μm thick InP cladding layers Zn-doped at 7×10^{17} cm^{-3} and Si-doped at 1×10^{18} cm^{-3} and 130 μm thick InGaAsP ($\sim$1.2 μm) confinement layers. The top laser has four 71 Å thick strained InGaAsP QWs separated by InGaAsP ($\sim$1.2 μm) barriers. The

bottom laser has four 74 Å thick strained InGaAsP QWs separated by InGaAsP ($\sim$1.2 μm) barriers. The tunnel junction consists of two 250 Å thick Si-doped, 5×10^{18} cm^{-3}, and Zn-doped, 5×10^{18} cm^{-3}, InGaAsP ($\sim$1.3 μm) layers. The laser material was characterized by fabricating gain-guided lasers 650 μm long and 50 μm wide. Figure 2.8 shows the light versus current density and spectral characterization. Again, it is evident from the spectra that two thresholds exist.

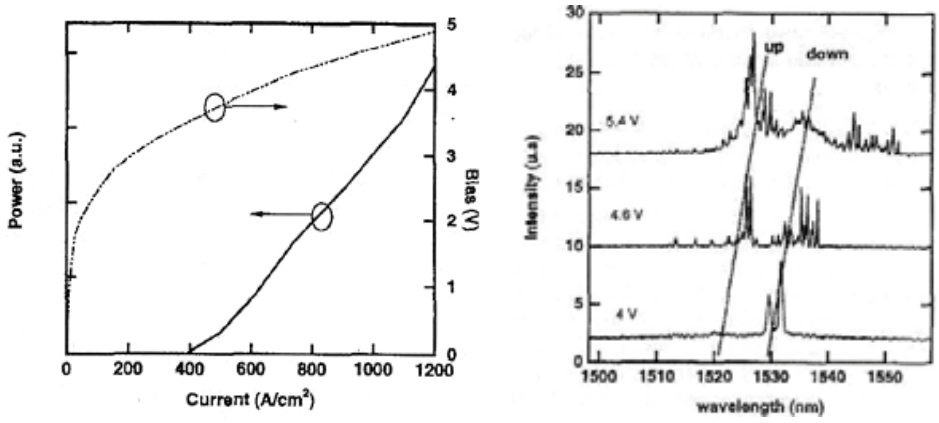


Figure 2.8: Light output vs. current density and spectral characterization for InGaAsP-based 650 μm long and 60 μm wide intercavity BCL [24].

2.2.5 University of Ulm. Researchers at the University of Ulm in Germany have incorporated an intracavity BCL structure into a VCSEL cavity [32]. This device is grown by MBE and the schematic diagram is shown in Figure 2.9. The p- and n-type mirrors are AlGaAs-GaAs DBR mirrors. The optical core is a 2λ cavity of an $Al_{0.4}Ga_{0.6}As$ core and embedded at the two outside anti-nodes are the active regions consisting of 80 Å thick $In_{0.2}Ga_{0.8}As$ QWs separated by 100 Å thick GaAs barriers. The tunnel junction is located in the center node and consists of two 100 Å thick $Al_{0.4}Ga_{0.6}As$ layers, one Si-doped at 5×10^{18} cm^{-3}, and the other C-doped at 5×10^{19} cm^{-3}. The location of the tunnel junction at the node of the standing wave pattern is to reduce free-carrier absorption. The structure is then fabricated into an oxide-aperture VCSEL. The top p-doped DBR layer was wet etched to form a mesa and the 300 Å thick AlAs layer was oxidized. A ring contact of p-ohmic Ti:Pt:Au metal layers was deposited and annealed on the mesa, and an n-ohmic

Ge:Ni:Au metal layers were deposited onto the entire backside of the wafer and annealed. The continuous-wave (CW) LI characteristics for a device with a 16 μm diameter OA at a cold finger temperature of 95 K is also shown in Figure 2.9. The I_{th} for this device is $\sim$14 mA and an $\eta_{d-device}$ of $\sim$1.2 was measured. However, the threshold voltage of $\sim$7 V was large compared to twice the bandgap voltage and is attributed to the tunnel diode.

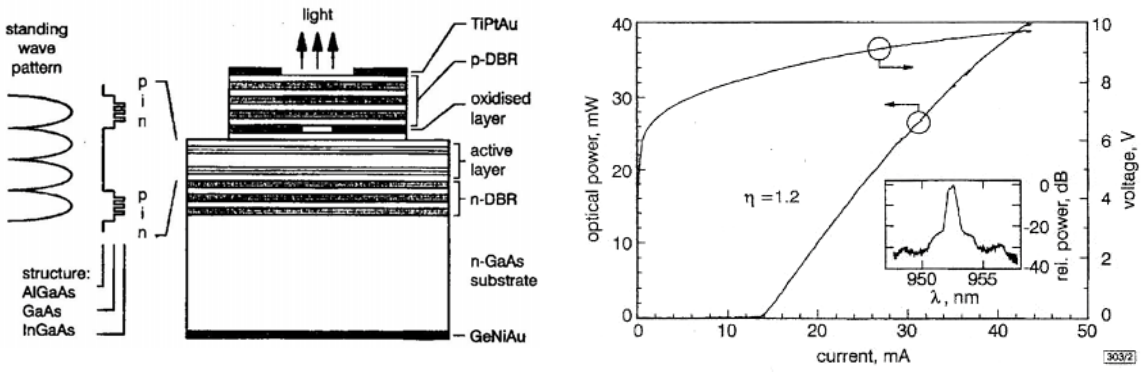


Figure 2.9: On the left is the schematic of Univ. of Ulm's 2λ intracavity BCL. The CW LI characteristics for an intracavity BCL with an OA diameter of 16 μm at 95 K is shown on the right. Inset is emission spectrum at 95 K [32].

2.2.6 Massachusetts Institute of Technology. Researchers at the Massachusetts Institute of Technology have demonstrated an intercavity CW room-temperature BCL [28]. The device is grown by gas-source MBE and the schematic is shown in Figure 2.10. The device consists of two identical laser junctions. The cladding layers are 0.75 μm InGaP lattice-matched layers with either Be doping or Si doping. The active region is a 220 nm core with a single 80 Å thick $In_{0.2}Ga_{0.8}As$ QW embedded in the center. The tunnel junction consists of two 250 Å thick GaAs layers with one layer heavily Si-doped and the other heavily Be-doped. The choice for this type of cladding layer is to avoid Be diffusion. AlGaAs layers are typically grown at higher temperatures where Be is known to diffuse into other layers. InGaP can be grown at lower temperatures and Be diffusion is greatly reduced. Figure 2.10 also shows the room-temperature CW LI operating characteristics. Again, two distinct thresholds are evident, indicative of an intercavity BCL. After the second threshold is crossed, the $\eta_{d-device}$ is measured to be $\sim$0.99.

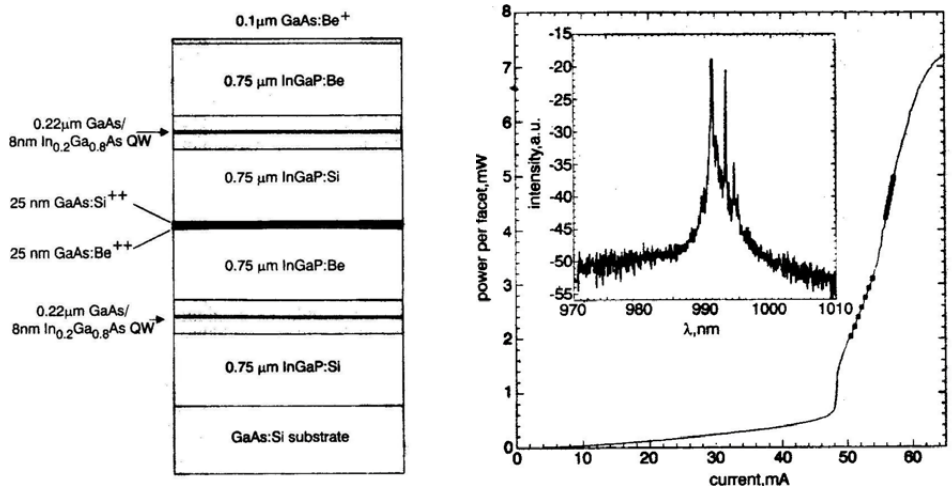


Figure 2.10: On the left is the schematic of the MIT intercavity BCL. CW LI characteristics for the intercavity bipolar cascade laser is on the right. Inset is the emission spectrum [28].

2.2.7 University of California at Santa Barbara. Researchers at the University of California at Santa Barbara (UCSB) are investigating AlInGaAs QW BCL structures operating at a wavelength $\sim$1.5 μm for telecommunication and eyesafe applications. UCSB has reported on the development of two different intracavity laser devices. The first device is a 1λ cavity edge-emitting structure with three active regions and two tunnel junctions [18] and the second device is a 2λ cavity VCSEL with three active regions and three tunnel junctions [17].

The first intracavity λ $\sim$1.5 μm AlInGaAs device was grown by MBE and 50 μm wide gain-guided lasers were fabricated. Figure 2.11 shows the edge-emitting structure with insets showing the active regions in relation to the mode and the active regions in relation to the tunnel junctions. Laser cavity lengths of 250 μm, 500 μm, 750 μm, and 1000 μm were cleaved and analyzed. Figure 2.11 shows plots of the LI, IV, and inverse η_d characterization.

The second intracavity λ $\sim$1.5 μm AlInGaAs device was grown by MBE and is a 2λ cavity VCSEL. Figure 2.12 shows the VCSEL structure. The interesting innovation in this device is the use of a third tunnel junction allowing the top 45 period AlInGaAs/AlInAs DBR mirror to be an n-doped DBR mirror instead of a p-doped DBR mirror. This reduces

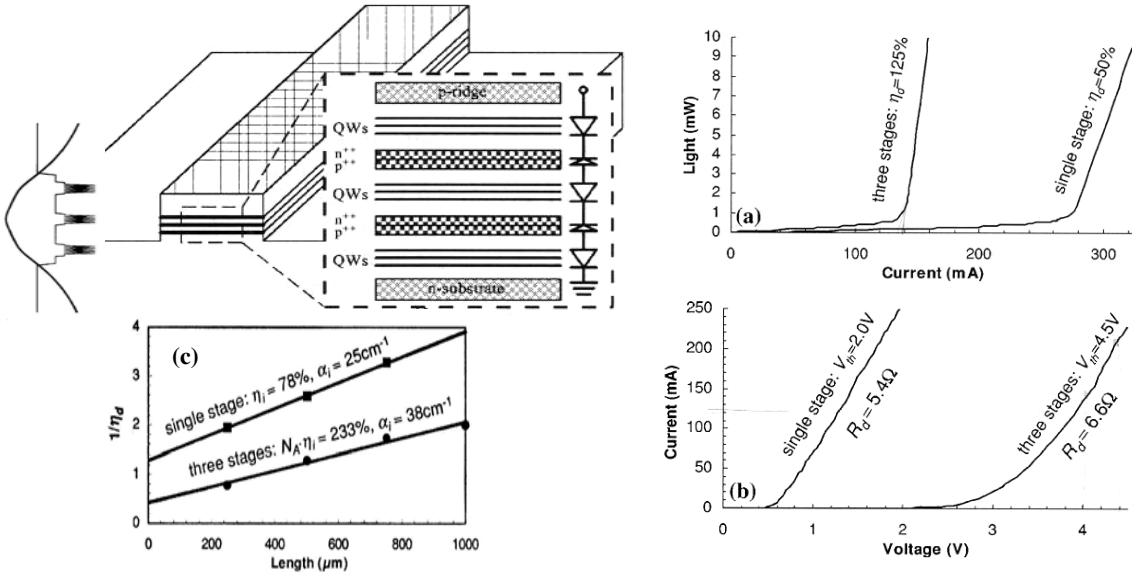


Figure 2.11: On the left is the schematic of the UCSB edge-emitting intracavity BCL. The leftmost inset indicates the active regions in relation to the mode. The right inset indicates the active regions in relation to the tunnel junctions. Characteristics for the intracavity BCL. a) Plot of LI for BCL and comparable single stage device. b) Plot of IV for BCL and comparable single stage device. c) Inverse η_d for BCL and comparable single stage device [18].

the free-carrier absorption significantly, by as much as a factor of two, if the tunnel junction free-carrier absorption is not factored in. The tunnel junctions are placed in the nulls of the standing wave pattern and the active regions are located in the peaks. The LI and VI characteristics for 25 μm, 50 μm, and 100 μm diameter devices are also shown in Figure 2.12. The devices were tested at room temperature with 1 μs pulses and a duty cycle of 0.1%.

2.3 Summary

This chapter has provided and overview of TJs and how they incorporate into semiconductor lasers to form BCLs. The TJ history, theoretical development, and applications have been discussed. The development of BCLs has been discussed illustrating numerous approaches (intercavity and intracavity edge-emitting BCLs and intracavity BC VCSELs) and material systems (GaAs and InP). This has formed the basis for the following research in this dissertation.

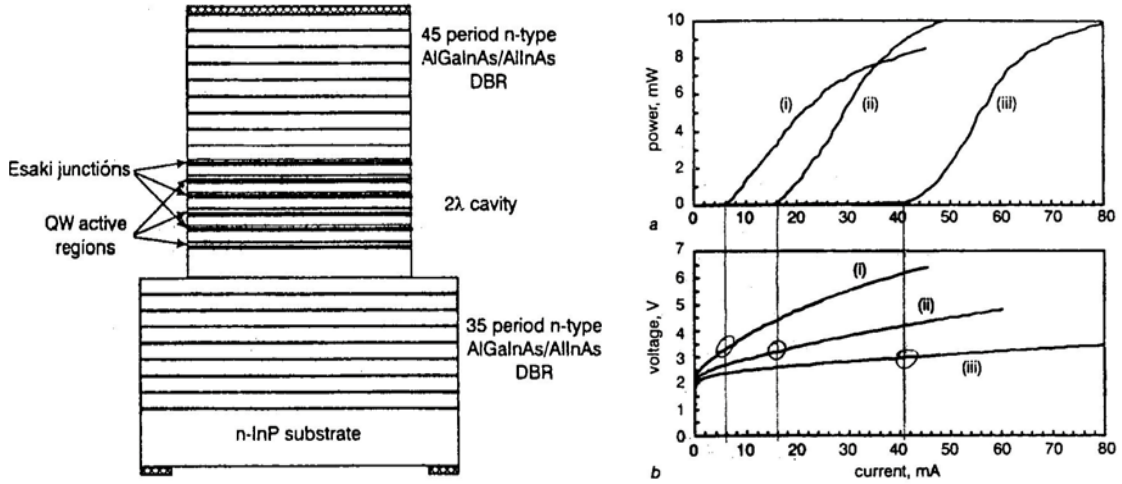


Figure 2.12: On the left is the schematic of UCSB's 2λ intracavity BC VCSEL structure. Operating characteristics for the structure with mesa diameters of: i) 25 μm, ii) 50 μm, and iii) 100 μm. The top is LI and the bottom is VI characterization [17].

III. Bipolar Cascade Laser Development

3.1 Introduction

BCLs show excellent potential for producing gain in RF photonic links [28], improving the efficiency of high-power diode lasers [14], and realizing multiple-color laser devices [12]. High-speed BCLs can be used as the direct-drive optical carrier for an RF photonic link system. The benefits of a BCL over a standard high-speed diode laser include an increased slope efficiency, yielding an increased device quantum efficiency, which can be greater than unity, and improved RF impedance matching, since the BCLs can be closely matched to the load impedance by engineering the number of epitaxially grown active region stacks.

Development of BCLs has been ongoing at the AFRL Sensors Directorate [37]. All device design and modeling, fabrication, and characterization was performed by the author. All of the MBE growth was accomplished by Mr. James Ehret of AFRL's Materials and Manufacturing Directorate (AFRL/MPLSM). This development has followed a strict systematic approach. The first step entailed modeling the tunnel junction doping levels and thicknesses, developing the growth techniques for Si δ-doping, and then growing, fabricating, and characterizing tunnel junction devices. Second, multiple-cavity multiple-color edge-emitting BCLs, multiple-cavity single-color edge-emitting BCLs, and finally, single-cavity single-color BCLs were grown, fabricated, and characterized. Third, BC light emitting diodes (LEDs) were investigated to optimize the microcavity prior to BC VCSEL growth. Finally, BC VCSEL structures were designed, grown, fabricated, and characterized. Investigation of these BC VCSEL devices included standard laser characterization prior to and after oxidation, as well as high-speed frequency modulation investigations, to extract frequency response, the -3 dB frequency, and the relaxation oscillation frequency.

3.2 Tunnel Junction Development

GaAs tunnel junctions are difficult to develop and very little technical detail has been reported in the literature, except from tandem solar cell research [1, 9]. In GaAs-based diodes and BCLs, a major difficulty is achieving high electron concentration in the n-doped

region. When Si is used as the n-dopant, it becomes amphoteric, where the silicon atom resides on the arsenic lattice sites (becoming a p-dopant) as well as the preferred gallium lattice sites (n-dopant), as the doping concentration increases beyond $\sim 5 \times 10^{18}$ cm^{-3}.

To model the doping concentrations required for GaAs-based TJs a temperature dependant model was developed that calculated electron and hole concentrations for a specifically doped layer and then combined the p-doped and n-doped layer to determine the built-in voltage and depletion width of the *p-n* junction. The desired depletion width, x_w was to be on the order of 100 Å so the TJ could be made with layer thicknesses as thin as 100 Å.

The model first calculates the temperature dependent bandgap energy using the Varshni relation [42]

$$E_{gap}(T) = E_{gap}(0) - \left(\frac{\alpha T^2}{T+\beta}\right) \tag{3.1}$$

where $E_{gap}(0)$ is the bandgap energy at zero Kelvin, α and β are the Varshni parameters, and T is the temperature in K. The effective density of states for the conduction band and valence band (defined in section 2.1.2, equations 2.4 and 2.5) are then calculated and the temperature dependent intrinsic carrier concentration is calculated by

$$n_i(T) = \sqrt{N_c(T)N_v(T)\exp\left(-\frac{E_{gap}(T)}{k_B T}\right)}. \tag{3.2}$$

The Fermi energy is then calculated by root solving the charge neutrality condition

$$n + N_a^- = p + N_d^+ \Longrightarrow n + N_a^- - p - N_d^+ = 0 \tag{3.3}$$

where n is the electron concentration, and p is the hole concentration with the following integral form

$$n = \int_{-\infty}^{\infty} f_n(E)\rho_e(E)dE = N_c F_{\frac{1}{2}}\left(\frac{F_n - E_c}{k_B T}\right) \tag{3.4}$$

and

$$p = \int_{-\infty}^{\infty} f_p(E)\rho_h(E)dE = N_v F_{\frac{1}{2}} \left(\frac{E_v - F_p}{k_B T} \right). \tag{3.5}$$

The integral in the carrier concentrations are Fermi-Dirac integrals and can only be solved numerically. The integrand is the product of the Fermi occupation probability, $f_n(E)$ for equation 3.4 and $f_p(E)$ for equation 3.5, respectively

$$f_n(E) = \frac{1}{1 + \exp\left(\frac{E - F_n}{k_B T}\right)} \tag{3.6}$$

and

$$f_p(E) = \frac{1}{1 + \exp\left(\frac{F_p - E}{k_B T}\right)}. \tag{3.7}$$

The carrier density of states, $\rho_e(E)$ for equation 3.4 and $\rho_h(E)$ for equation 3.5

$$\rho_e(E) = \frac{1}{2\pi^2} \left(\frac{2m_e^*}{\hbar^2} \right)^{\frac{3}{2}} (E - E_c)^{\frac{1}{2}} \tag{3.8}$$

and

$$\rho_h(E) = \frac{1}{2\pi^2} \left(\frac{2(m_{hh}^* + m_{lh}^*)}{\hbar^2} \right)^{\frac{3}{2}} (E_v - E)^{\frac{1}{2}}. \tag{3.9}$$

Where E_c is the conduction band energy and E_v is the valence band energy.

N_d^+ is the ionized donor concentration, and N_a^+ is the ionized acceptor concentration. N_d^+ and N_a^- are determined with the following relations

$$N_d^+ = N_d \left[1 - \frac{1}{1 + \frac{1}{g_d} \exp\left(\frac{E_d - E_F}{k_B T}\right)} \right] \tag{3.10}$$

and

$$N_a^- = \frac{N_A}{1 + g_a \exp\left(\frac{E_a - E_F}{k_B T}\right)}. \tag{3.11}$$

Where g_d and g_a are the donor and acceptor degeneracies, respectively, E_d and E_a are the donor and acceptor binding energies, respectively, and E_F is the Fermi energy. Table 3.1 lists the parameters used for GaAs and the dopants.

Table 3.1: Parameters for modeling the temperature dependant doping concentrations for GaAs *pn* junctions. [5, 42]

Parameter	GaAs
$E_{gap}(0)$	1.519 eV
α	5.405 10^{-4} eV/K
β	204 °K
m_e^*	0.0665m_o
m_{hh}^*	0.5m_o
m_{lh}^*	0.087m_o
ε_r	13.1ε_o
g_a	4
g_d	2
Donor	Si
E_d	5.8 meV
Acceptor	C
E_a	26 meV

After determining the Fermi energy for a given donor concentration the carrier concentration is calculated using the formulas for n or p, shown above. After carrier concentrations for both n-type and p-type donor concentrations are calculated the built-in voltage is determined by

$$V_o = \frac{F_n - F_p}{q} \tag{3.12}$$

and the zero-bias depletion width, is determined by

$$x_w = (N_d + N_a)\sqrt{\frac{2\varepsilon_r \varepsilon_o V_o}{q N_a N_d (N_d + N_a)}}. \tag{3.13}$$

Figure 3.1 shows the temperature-dependant carrier concentrations for a) Si-doped GaAs and b) C-doped GaAs at the indicated doping concentrations. Due to the smaller binding energy for Si it is evident that at high doping concentrations, $N_d > 10^{17}$ cm^{-3}, not all of the dopants are ever activated. For the Si doping level of 10^{19} cm^{-3} the activated carriers are an order of magnitude less at room temperature. For the C-doped GaAs the inefficient doping activation only begins to be evident at concentrations of 10^{19} cm^{-3} and higher, but not as significantly as the Si-doped GaAs. This will allow for a TJ with nearly an order of magnitude larger p-doped layer than the n-doped layer. This is particularly attractive when one considers the electron mobility is much greater than the hole mobility. With a significantly greater number of holes the conduction band electrons have many more states to tunnel into in the valence band.

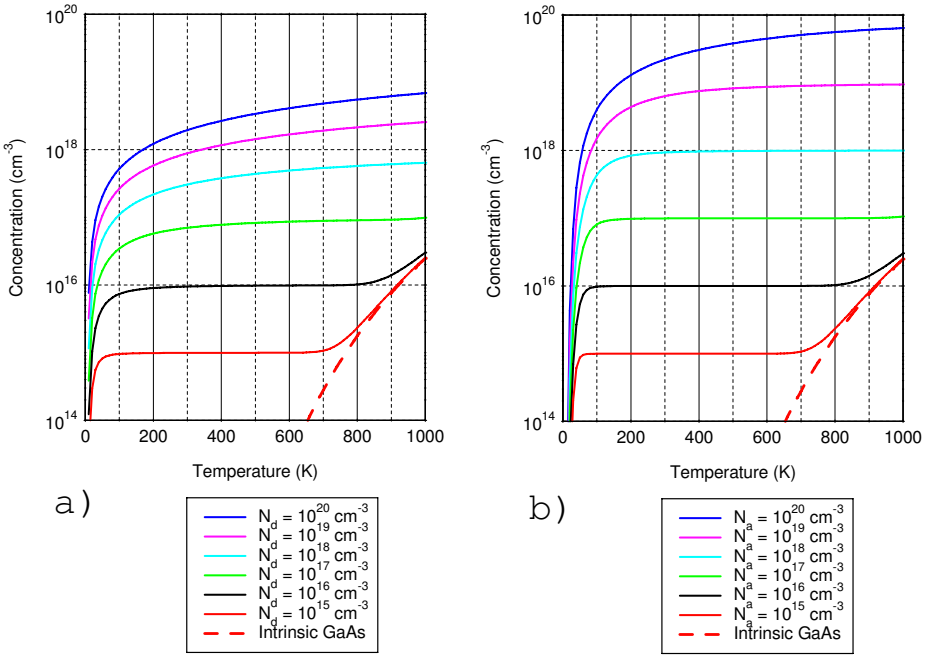


Figure 3.1: Temperature dependant carrier concentrations for GaAs. a) illustrates Si-doped GaAs and b) illustrates C-doped GaAs at the indicated doping concentrations.

Figure 3.2 shows the temperature-dependant depletion width with various n and p doping concentrations. At lower doping concentrations the depletion widths are quite large, > 1 μm. Not until the concentrations for both layers are greater than 10^{17} cm^{-3} do the depletion widths become small enough for incorporation into a TJ structure with the most

desirable doping concentrations being greater than 10^{19} cm^{-3}. This doping level is readily achievable for the p dopant when C is used. C-doping can typically reach mid 10^{20} cm^{-3} before material quality becomes an issue. As mentioned at the beginning of this section, Si becomes amphoteric at concentrations greater than 5×10^{18} cm^{-3} so the δ-doping technique was used to increase the effective doping concentration of the Si-doped n-layer of the TJ.

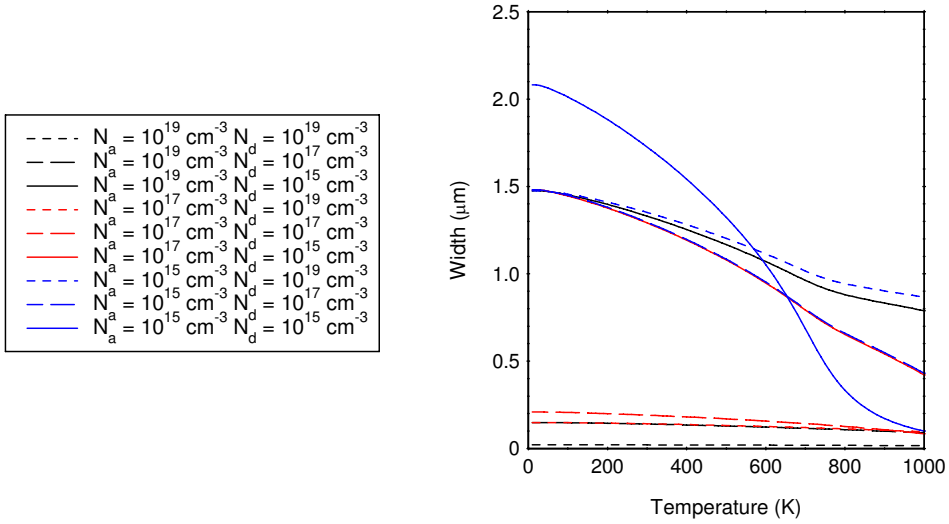


Figure 3.2: Temperature dependant depletion width calculations for GaAs pn junction.

To evaluate tunnel junction performance, numerous samples were designed by the author, grown by AFRL/ML in a Varian Gen II MBE system, then fabricated and characterized by the author. In all of these structures, a 1000 Å thick GaAs:Si (5×10^{18} cm^{-3}) buffer layer was grown on an n-doped GaAs substrate held at 600 °C. The Si source temperature was set at 1300 °C for the entire growth. After the buffer layer was completed, the substrate temperature was lowered to 510 °C to replicate the growth conditions of InGaAs quantum wells. The n-layer of the tunnel junction was formed by growing ten 10 Åthick Si-doped GaAs (4×10^{18} cm^{-3}) layers separated by nine 25 s (or 40 s) Si δ-doped "layers," which are simply growth delays while the Si shutter is open for the time indicated. The 25 s Si δ-doping resulted in an effective doping concentration of 2×10^{19} cm^{-3} as measured using Hall and electro-chemical capacitance-voltage techniques. A 600 Åthick GaAs:C (5

or 8×10^{18} cm^{-3}) p-layer of the tunnel junction was then grown. Table 3.2 summarizes the tunnel junction thickness and concentration values used in this study.

The tunnel junction devices were processed using standard photolithography techniques into square structures of varying dimensions, 50 μm, 100 μm, 200 μm, 400 μm, 800 μm, and 1600 μm. The top contact metal was an evaporated Ti:Pt:Au (300 Å:500 Å: 3500 Å) metal contact which was annealed at 410 °C for 15 s. No mesa isolation was used because the TJ devices were very large and lateral diffusion would have been negligible. The backside was evaporated with a Ni:Ge:Au:Ni:Au (50 Å:170 Å:330 Å:150 Å: 3000 Å) metal layer composition and alloyed at 410 °C for 15 s. IV characteristics were obtained using a probe station and Techtronics curve tracer.

Table 3.2: Details of tunnel junction doping parameters. The p-doped layers are 600 Å thick and the total n-layer thickness is 100 Å consisting of ten 10 Å thick layers doped at 4×10^{18} cm^{-3} and nine δ-doping interrupts.

TJ	p-doping Concentration (10^{19} cm^{-3})	n_{eff}-doping Concentration (10^{19} cm^{-3})	Si δ-doping Interrupt (s)	Si Sheet Concentration (10^{12} cm^{-2})
#1	8	2.0	25	8.8
#2	8	0.8	40	5.5
#3	5	0.8	40	5.5
#4	5	2.0	25	8.8

Figure 3.3 shows the room-temperature IV characteristics of four 200 $\times$ 200 μm^2 tunnel junction devices [37]. Carbon doping concentration clearly influences the onset of NDR in the tunnel junction device. These results also demonstrate the importance of Si δ-doping parameters on the peak-to-valley characteristics of NDR; Si δ-doping for too long results in the silicon becoming an amphoteric dopant. The results from sample TJ #1 clearly demonstrates strong evidence via NDR, more importantly, a steep reverse-biased slope, required for effective BCL operation. The steeper the reverse-biased slope the lower the resistance is for the series connector between two cascade lasers in a BCL.

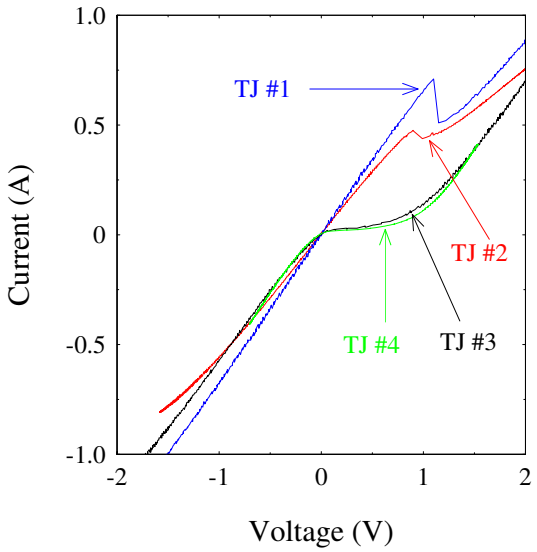


Figure 3.3: Room-temperature IV characterization for four different 200 μm by 200 μm tunnel junction devices. The TJ number corresponds to the TJ number in Table 3.2 [37].

3.3 Multiple-Cavity Multiple-Color Bipolar Cascade Lasers

Two-cavity two-color BCLs were developed to rapidly verify the independent lasing of the two lasers. With a two-cavity single-color BCL, the easiest indicator that both lasers are lasing is the kink in the LI curve further verified by differential analysis of the LI information. The single-color BCL facet could be imaged to indicate independent lasing but this adds greater complexity to the test setup. With a two-color BCL, the LI information is readily measured as in a single-color device, and the spectral operation as a function of current is easily obtained.

The BCLs were designed by the author and grown by AFRL/ML in the same MBE system where the TJ devices were grown. The edge-emitting laser structures used in the BCLs were previously designed structures with very good operating characteristics [15, 35, 41]. The BCL designs consist of two epitaxially stacked lasers, each with 1 μm $Al_{0.6}Ga_{0.4}As$ n- and p-cladding layers, Si- and C-doped respectively to 4×10^{18} cm^{-3}, 2000 Å undoped $Al_{0.2}Ga_{0.8}As$ ternary electrical confinement layers, 100 Å GaAs barriers, and either three 80 Å $In_{0.20}Ga_{0.80}As$ QWs for emission at $\sim$980 nm or three 50 Å $In_{0.20}Ga_{0.80}As$ QWs for emission at $\sim$950 nm. These lasers were separated by a reverse-

biased tunnel junction consisting of a 100 Å Si δ-doped layer, described above, and either a 600 Å or 100 Å C-doped layer doped at 5×10^{19} cm^{-3} or 8×10^{19} cm^{-3}. The 600 Å C-doped layer was used to replicate the tunnel junction device development and the 100 ÅC-doped layer thickness was used to evaluate the effect of thickness reduction on laser device properties.

The BCLs were fabricated by the author, using standard photolithographic techniques, into gain-guided lasers with varying device widths and lengths. Appendix A provides the detailed process follower for fabricating gain-guided lasers. The BCLs were photolithographically patterned with stripe widths of 20 μm, 40 μm, 60 μm, 80 μm, and 100 μm. The top metal, consisting of the same Ti:Pt:Au used for the TJ devices, was evaporated and annealed at 410 °C for 15 s. The BCL substrates were then thinned to a a final thickness of $\sim$100 μm and the backside Ni:Ge:Au:Ni:Au metal, used for the TJ devices, was evaporated and annealed. The BCL samples were then cleaved into 1 cm laser bars with cavity lengths of 200 μm, 250 μm, 330 μm, 400 μm, 500 μm, 660 μm and 800 μm.

Room-temperature CW and pulsed LI characterization and spectral analysis were performed on all growth structures. The CW LI characterization system consisted of a probe station, an ILX 9072 Laser Parameter Analyzer (LPA), and a computer for LPA control and data acquisition.

The pulsed LI characterization system consisted of a probe station, an ILX 3811 Pulsed Current Source, two Stanford Research Corp. gated integrator and boxcar averaging modules and a computer interface module, a Si photodetector with a transimpedance amplifier, and a Techtronix four channel oscilloscope.

Figure 3.4 demonstrates AFRL's first room-temperature CW operating BCL (BCL #1). This device is a 20 μm wide by 500 μm long laser cavity. This multiple-cavity BCL had a tunnel junction with a 600 Å thick C-doped layer at 5×10^{19} cm^{-3}. The bottom laser is seen to lase first at $\sim$960 nm with a threshold current of 144 mA. The second laser's threshold occurs at 247 mA with a peak lasing wavelength $\sim$990 nm. The voltage is more than twice the normal operating voltage for a standard InGaAs triple QW device, as illustrated by the

light blue curve in Figure 3.4, indicating losses due to the tunnel junction on the order of 0.75 V. As the current increases, there is a large red shift in the output wavelength due to junction heating.

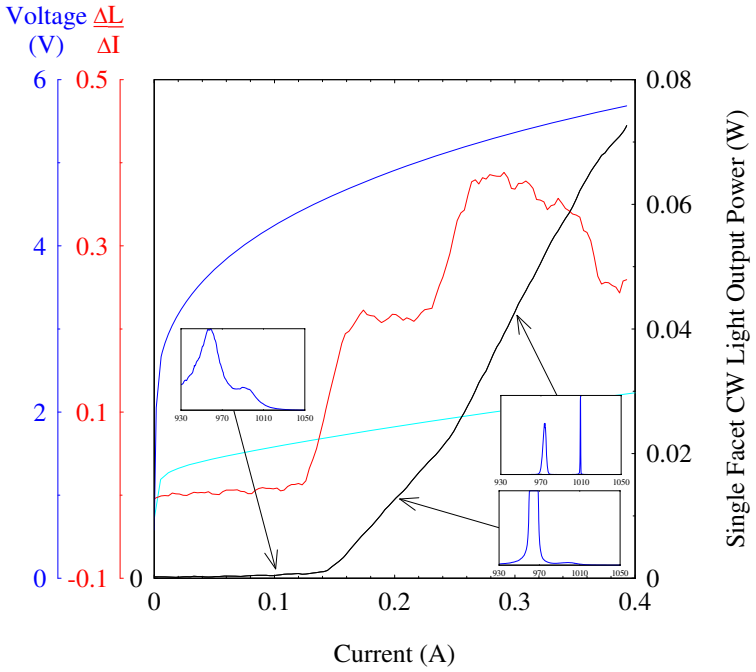


Figure 3.4: LI, VI and $\Delta L/\Delta I$ (W/A) characteristics of the first AFRL edge-emitting two-cavity two-color BCL. Normalized spectral analysis at 100 mA, 200 mA, and 300 mA verifies the independent lasing evolution of the two-color device. The light blue curve is the VI for a standard InGaAs triple QW laser.

Figure 3.5 shows a comparison of the LI and VI characteristics for the three BCL devices studied and Table 3.3 provides a summary of the BCL layer characteristics. The stripe geometry was 20 μm wide by 500 μm long for all of the devices. The first BCL (BCL #1) is the same device described in the previous paragraph and in Figure 3.4. The next two multiple-cavity, multiple-color BCLs (BCL #2 and BCL #3) were grown to provide a systematic study of the effect of changing the p-doped layer of the tunnel junction to either a 600 Åor 100 Å C-doped layer doped at 8×10^{19} cm^{-3}. This investigation was necessary because during the TJ development a larger 600 Åthick layer was necessary to avoid metal diffusion during the anneal of the TJ devices.

Table 3.3: Details of BCL parameters. All other layer parameters are the same for each sample grown.

BCL	p-doping (10^{19} cm^{-3})	p-thickness Å
#1	5	600
#2	8	600
#3	8	100

The p-doping concentration, in both BCL # 2 and BCL # 3, had the better performing tunnel junction characteristics, as shown in Figure 3.3. As Figure 3.5 shows, there is a dramatic reduction in operating voltage for both of these devices compared to BCL #1. Increasing the p-doping concentration significantly improves device operating voltage performance. Reducing the p-doped thickness of the tunnel junction has little or no effect on the voltage performance with minimal effect on threshold current. The use of this layer is important for making single-cavity BCLs because we desire the smallest possible tunnel junction layer thickness.

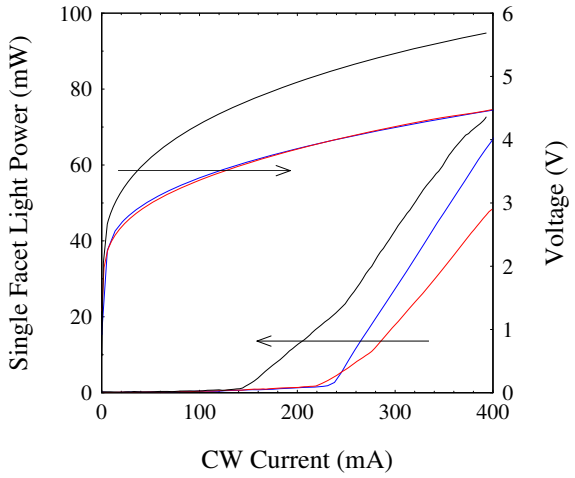


Figure 3.5: Room-temperature comparison of LI and VI operating characteristics for three BCL devices studied. Device dimensions are all 20 μm wide by 500 μm long. The black lines are BCL #1, the blue lines are BCL #2, and the red lines are BCL #3 [37].

3.4 Multiple-Cavity Single-Color Bipolar Cascade Lasers

Figure 3.6 demonstrates the operation of a two-cavity single-color BCL. This device was used to quantify the device differential quantum efficiency, $\eta_{d-device}$, which could not be effectively quantified because of the two colors of emission and the uncertainty of the amount of output coming from each active region. The $\eta_{d-device}$ for this sample was 1.015 under pulsed conditions of a 1 μs pulse with a 1% duty cycle. A two-cavity InGaAs device is compared with a standard triple quantum well diode laser developed previously [41]. The standard diode has a very high $\eta_d > 0.75$. Whereas the first stage of the BCL exhibits a lower $\eta_d \sim 0.56$. This is due to the greater complexity of two complete lasers and a reverse-biased TJ monolithically connecting the lasers.

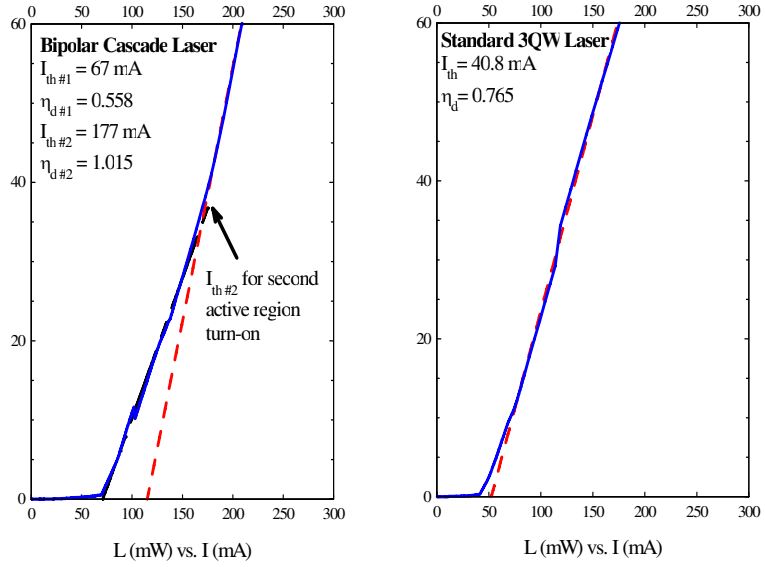


Figure 3.6: Two-cavity single-color BCL. This BCL device on the left details how a device quantum efficiency greater than 1 can be achieved. After the second threshold an η_d of 1.015 is measured. The device on the right is a standard triple QW laser developed previously [41].

3.5 Single-Cavity Single-Color Bipolar Cascade Lasers

$\frac{\lambda}{2}$ single-cavity single-color edge-emitting lasers were designed and investigated for single spatial (transverse and lateral) optical mode operation. These samples did not ex-

hibit uniform voltage or lasing characteristics. Figure 3.7 shows the pulsed operation of a single-cavity single-color device. This device never operated in CW mode, but the VI characteristics were identical from 0 - 300 mA. The pulsed "lasing" occurred at currents greater than 300 mA; however, it is obvious that instabilities in the device are evident in the VI trace. It became evident that the close proximity of the tunnel junctions with the InGaAs active regions, within a $\frac{\lambda}{2}$ cavity, was going to be very difficult to overcome. The decision was made to incorporate these tunnel junctions and multiple active regions within an oxide aperture VCSEL structure to achieve a single-mode laser.

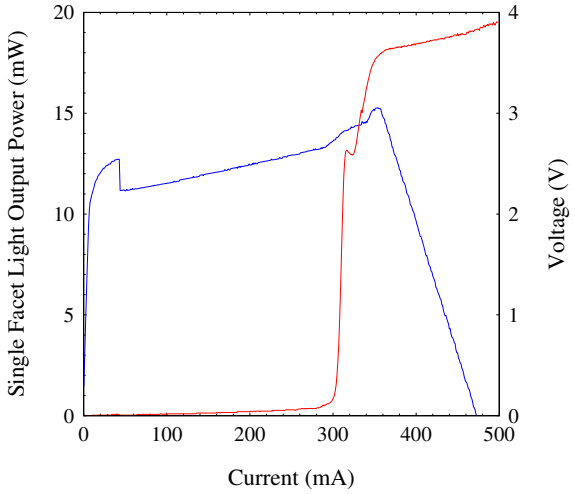


Figure 3.7: Unsuccessful demonstration of a single-color single-cavity edge emitting BCL. Voltage instabilities in both pulsed and CW operation at ∼40 mA and unstable light output emphasized the conclusion that single spatial mode emitters would have to be BC VCSELs.

3.6 Summary

This chapter has detailed the development of the high-quality GaAs-based TJ devices and the incorporation of those TJ material layers to monolithically integrate two lasers into a single edge-emitting BCL. The systematic process of developing, demonstrating, and improving a multiple-cavity multiple-color intercavity edge-emitting BCLs to verify independent laser operation was first discussed. The second step in the systematic approach, was to demonstrate the multiple-cavity single-color intercavity edge-emitting BCL to quantify

the improved slope and differential quantum efficiencies. Finally, the unsuccessful demonstration of a single-cavity single-color intracavity edge-emitting BCL verified the necessity to incorporate the BCL structure into a VCSEL structure to develop a single-cavity single-color intracavity for single optical mode operation.

IV. Bipolar Cascade Vertical-Cavity Surface-Emitting Lasers

4.1 Introduction

The AFRL Sensors Directorate and Materials & Manufacturing Directorate have been successfully designing and growing GaAs-based VCSELs for Air Force applications since the mid 1990s. The incorporation of multiple active regions into a VCSEL structure is a complicated endeavor because it significantly increases device growth times. These long growth times introduce drift considerations in the growth rates, material layer composition, and combinations of both. As discussed previously in Chapter III, a migration to a VCSEL structure rather than an edge-emitting structure is required for single-spatial mode emission in a BCL incorporating more than two stages. This chapter presents details on the design and fabrication of such BC VCSELs to meet the demands of such a device to be employed as a direct-drive laser for use in an RF-Link system.

The methodology employed in the development of the BC VCSELs studied in this dissertation is as follows: (1) Design a $\frac{5}{2}\lambda$ microcavity that includes a three-QW AR, a TJ, and an OA, then fix the microcavity to develop a modular format to rapidly develop designs for simulation. (2) Model, grow, fabricate, and characterize BC LEDs to determine the best microcavity to incorporate into a BC VCSEL structure. This avoided the long growth times, as well as provided a rapid prototype to investigate. (3) Grow, fabricate, and characterize high-speed BC VCSELs. Note, semiconductor modeling is not included in the BC VCSEL characterization. AFRL and AFIT have semiconductor modeling software capable of investigating BC structures that require quantum mechanical tunneling in simple devices like BC LEDs but do not presently have the more sophisticated software for BC VCSELs.

4.2 Bipolar Cascade Vertical-Cavity Surface-Emitting Laser Cavity Design

The first step in the BC VCSEL design was to determine the cavity, resonance of a $\frac{5}{2}\lambda$ cavity placing the triple quantum well AR in a intensity resonance antinode, and the TJ and OA in a intensity resonance node. The cavity designs were created using in-house developed code. These design software routines allowed for rapid development of numer-

ous BC VCSEL structures. Placing the three functions (AR, TJ, and OA) with the required material compositions and thicknesses included into the microcavity yielded a 6950 Å thick microcavity. To rapidly model different BC microcavity designs, the microcavity was divided into modules. Since the microcavity is a $\frac{5}{2}\lambda$ cavity, nine $\frac{\lambda}{4}$ modules, with a thickness of 695 Å and two $\frac{\lambda}{8}$ modules, with a thickness of 347.5 Å were constructed. The two $\frac{\lambda}{8}$ and six of the $\frac{\lambda}{4}$ modules consisted of undoped GaAs. The three remaining $\frac{\lambda}{4}$ modules were designed to be an AR, TJ, and OA module. Figure 4.1 is a schematic illustrating the modular structure for a $\frac{5}{2}\lambda$ microcavity. The AR module consisted of a 127.5 Å thick undoped GaAs layer, three 80 Å thick $In_{0.2}Ga_{0.8}As$ QWs separated by two 100 Å thick GaAs barriers, and another 127.5 Å thick undoped GaAs layer. The TJ module consisted of a 147.5 Å thick undoped GaAs layer, the 400 Å thick GaAs TJ, and another 147.5 Å thick undoped GaAs layer. The OA module consisted of a 17.5 Å thick undoped GaAs layer, a 180 Å thick $Al_xGa_{1-x}As$ graded layer with x increasing from 0.1 to 0.9, the 300 Å thick $Al_{0.98}Ga_{0.02}As$ OA, a 180 Å thick $Al_xGa_{1-x}As$ graded layer with x decreasing from 0.9 to 0.1, and another 17.5 Å thick undoped GaAs layer.

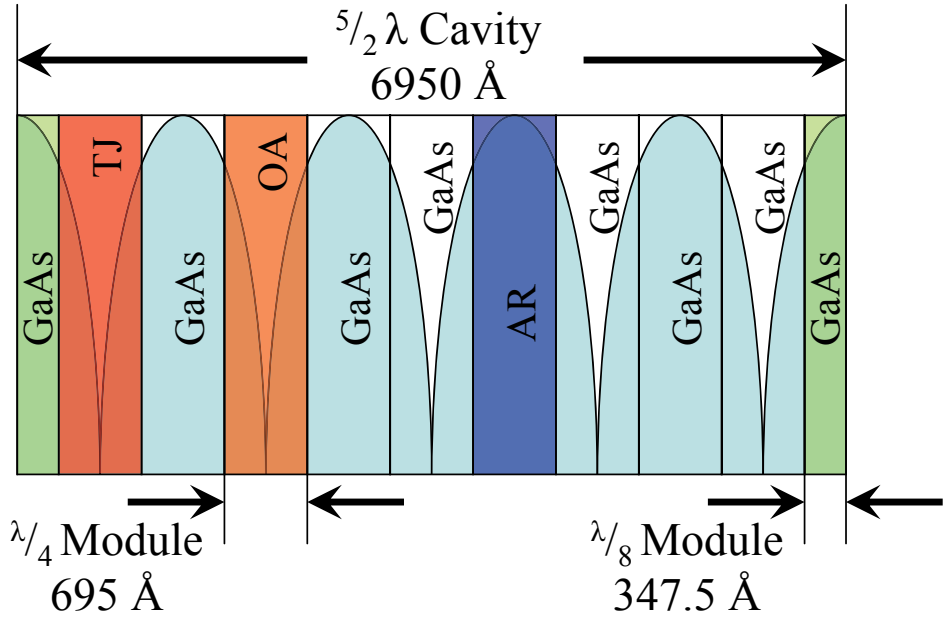


Figure 4.1: Schematic of the modular design of a $\frac{5}{2}\lambda$ microcavity. The intensity resonance profile is illustrated in light blue. There are six GaAs $\frac{\lambda}{4}$ (uncolored) and two $\frac{\lambda}{8}$ (green) modules, and one module of TJ (red), OA (orange), and AR (dark blue).

With this modular construction, the placement of each function could be quickly implemented. No changes with the GaAs and AR modules were ever required except for node and antinode (especially for the AR) placement within the microcavity. For the TJ module, care was required to ensure the hole injector, the p-doped TJ layer, was always placed nearest the AR, as well as ensuring the module was over a node. For the OA module, care was required to ensure the doping was appropriate for its placement and the module was over a node. For example, if the OA module is located between the AR and the hole-injecting TJ modules, the OA within the module must be p-doped.

Figures 4.2 a) and b) are full designs for the standard *p-i-n* and 1-stage BC VCSEL structures with the OA placed in the location where it can be either p-doped or undoped. All structures, *p-i-n*, 1-, 2-, and 3-stage, have 26.5 mirror pairs for the bottom DBR reflector and 15 mirror pairs for the top DBR reflector. The first structure, Figure 4.2 a), is a "standard" *p-i-n* VCSEL with the active region and undoped OA in the same location of the field intensity profile as the BC VCSELs. Figure 4.2 b) is a 1-stage BC VCSEL with both of the DBR mirror stacks Si-doped. The tunnel junction is in the node nearest the top DBR to act as the hole injector for this structure and the OA is in the next adjacent node. The 2- and 3-stage designs are identical to the 1-stage design except the microcavity is repeated two and three times, respectively. The blue traces are the layer index profiles; the red traces are the field intensities; and the black traces are normalized power densities. The power density is developed throughout the entire device by considering absorbed and "generated" top and bottom emitted powers, and integrating them with the field - index product over all of the layers. The "normalized" power density traces have been scaled to fit on the intensity axis. The "zero" axis is set to be two on the intensity axis for ease in viewing. This power density calculation provides valuable insight into the number of QWs that can be used within a resonance antinode.

Figure 4.3 shows zoomed-in views of the microcavity design for a) a *p-i-n* VCSEL, b) a 1-stage BC VCSEL, c) a 2-stage BC VCSEL, and d) a 3-stage BC VCSEL. Using a three-quantum well active region centered in a field intensity antinode results in less than a 10% decrease in power of the outer QWs compared to the middle QW. These designs show

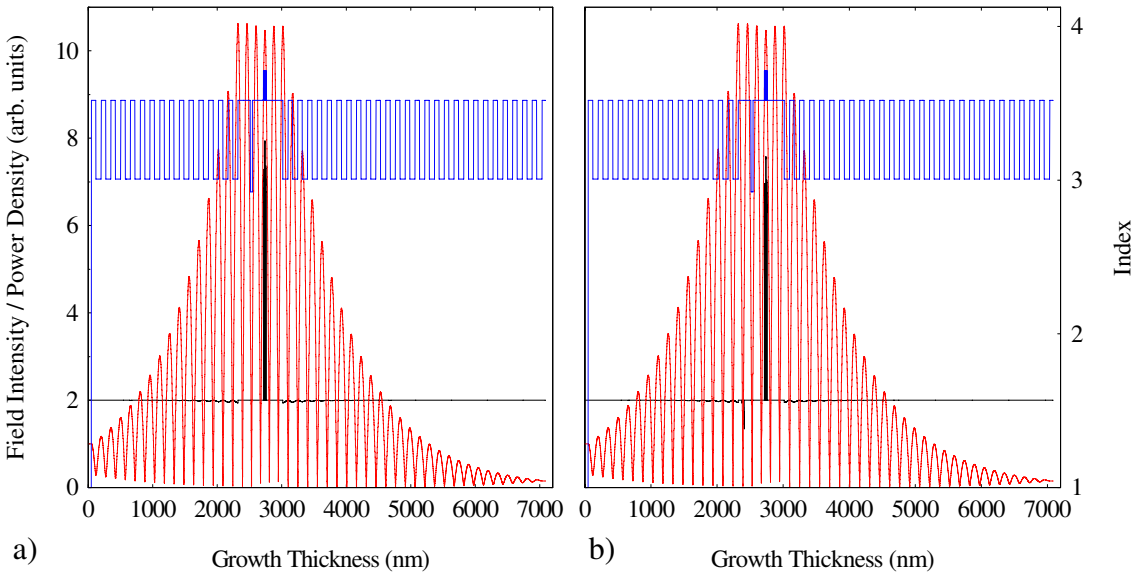


Figure 4.2: Standard and BC VCSEL designs a) is the standard *p-i-n* VCSEL and b) is the 1-stage BC VCSEL. The blue traces are the layer index profiles; the red traces are the electric field intensities; and the black traces are power densities.

an interesting improvement opportunity to reduce device losses. The p-doped tunnel junction layer shows a large loss in the power density. Shifting the TJ slightly to the left so the higher loss p-doped TJ layer is closer to the cavity node will reduce scattering losses. While it would be expected the n-doped TJ layer would exhibit increased scattering losses, these losses will be significantly less because the p-doped TJ layer has nearly an order of magnitude higher doping than the n-doped TJ layer. Also, per decade of doping, the p-doping losses are much larger than n-type losses. Combined with the higher doping concentration, a compounded loss effect that can really negatively impact device performance is achieved.

4.3 Bipolar Cascade Light Emitting Diode Modeling

With the definition of the BC VCSEL microcavity complete, the modeling of BC LEDs was initiated. Investigating BC LEDs instead of BC VCSELs initially provided a first step that disentangled the physics of the microcavity in BC VCSELs from the additional complications that result from laser operation in a similar BC VCSEL structure. Semiconductor and optoelectronic modeling was accomplished with APSYS software from

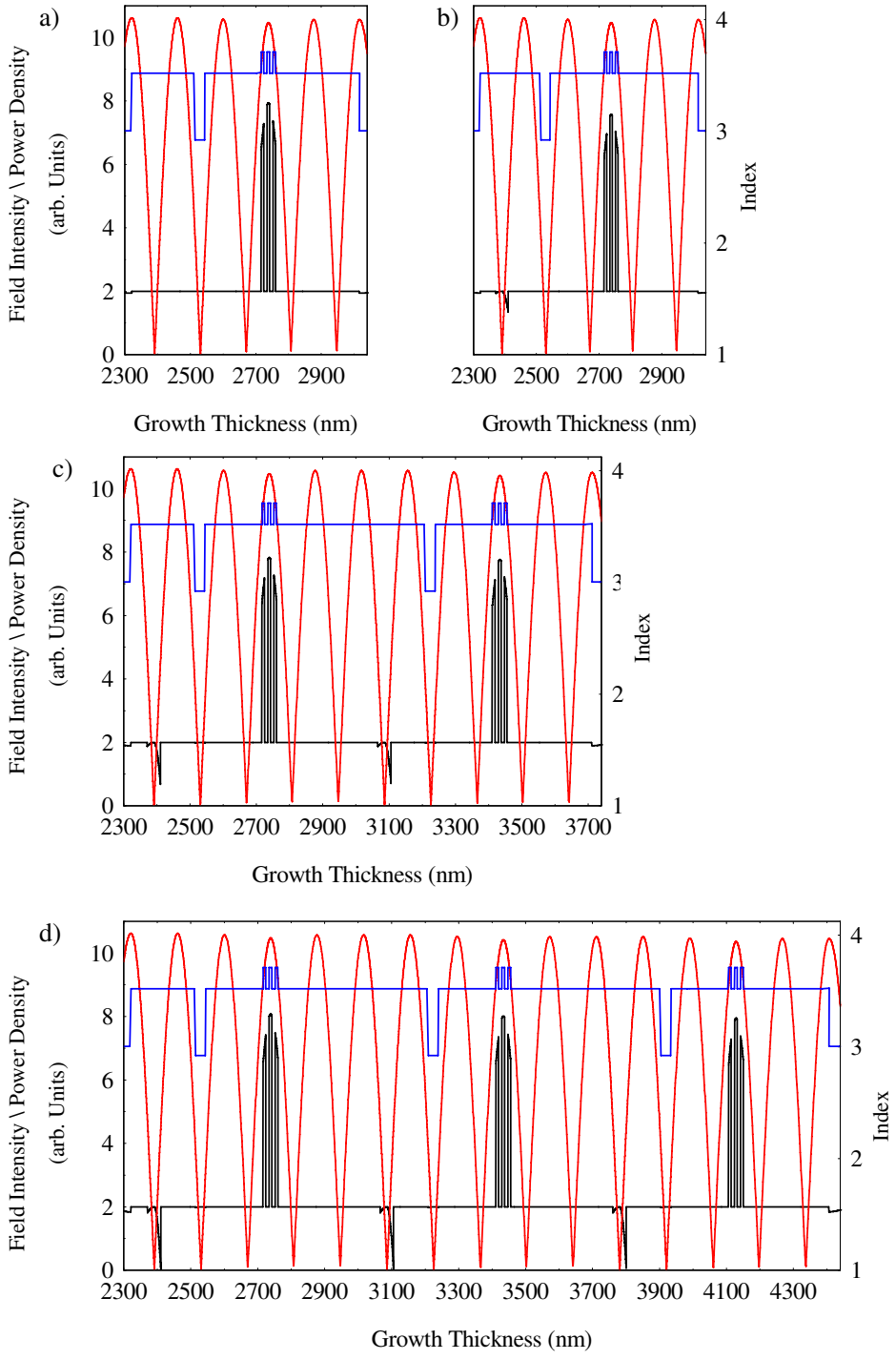


Figure 4.3: Standard and BC VCSEL microcavity designs a) is the standard *p-i-n* VCSEL, b) the 1-stage BC VCSEL, c) the 2-stage BC VCSEL, and d) the 3-stage BC VCSEL. The blue traces are the layer index profiles, the red traces are the electric field intensities, and the black traces are a power density plot.

Crosslight and included, at a minimum, band structure, VI, and LI simulations for LED structures. This software allowed for the investigation of LED structures with applied bias and injected current. Unbiased and biased band diagrams were developed for the *p-i-n* LED, and 1-, 2-, and 3-stage BC LEDs with undoped, n-type, and p-type OAs. VI and LI characteristics were also modeled and will be discussed in Section 4.4.3.

Figure 4.4 is the band diagram for the *p-i-n* LED with an n-doped OA. Figures 4.5, 4.6, and 4.7 are band diagrams comparing 1-stage , 2-stage, and 3-stage BC LEDs, respectively, with a) undoped, b) n-doped, and c) p-doped OAs. For the p-doped designs the order of the microcavity was changed so the hole injector was always on the valence band side of the QWs. For all these designs, the first 0.5 μm is the n-doped GaAs substrate. For the BC LEDs, the microcavity is sandwiched between 0.2 μm thick layers of n-doped GaAs, and for the *p-i-n* LED, the microcavity is sandwiched between a 0.2 μm thick n-doped GaAs layer next to the GaAs substrate and a 0.2 μm thick p-doped GaAs layer on top.

By n-doping the OA, several benefits were immediately identified: (1) n-doping the OA dramatically reduced the required potential to flatten the bands. For a 1-stage device, the reduction was greater than 0.75 V. (2) The electron barrier in the conduction band was eliminated, thereby allowing more electrons to fill the quantum wells. (3) A hole barrier in the valence band was created, allowing greater hole accumulation around the QW region. This effect has not been discussed in the literature until this research reported it [39].

The improvements that are readily apparent by using a p-doped OA were (1) the increased region for hole accumulation in the valence band and (2) an electron barrier in the conduction band. Since electron mobility is significantly greater than hole mobility, the slight increase in the conduction band slope is greatly offset by the capability to accumulate a significantly greater number of holes in the valence band.

These diagrams provide tremendous evidence for p-doped OAs to significantly improved BC emitter performance. Comparing the band diagrams of an n-doped OA structure to a p-doped OA structure at 0 V and at a bias of 3 V yields several conclusions: (1) At 3 V, the p-doped OA has a 0.75 eV electron barrier in the conduction band, whereas in the

n-doped OA, there is nothing to restrict electrons not captured by the QWs from continuing on and dropping down into the next stage. This is detrimental to the initial stage because, as those electrons travel to the next stage, they are restricting hole generation because fewer valence band electrons in the first stage are able to tunnel into the conduction band of the subsequent stage. (2) At the 50 mA bias, the p-doped OA tunneling region is $\sim$0.5 eV and the n-doped OA tunneling region is $\sim$0.1 eV. This higher region increases the number of states to which valence band electrons can tunnel and become conduction band electrons for subsequent stages.

4.4 Bipolar Cascade Light Emitting Diodes

4.4.1 Introduction. Single-cavity BC VCSELs and LEDs have shown great promise for increasing device slope efficiency and differential quantum efficiency by epitaxially connecting in series ARs with reverse-biased TJs [17, 21]. As with conventional *p-i-n* junction VCSELs, a common design feature of the BC variety is an OA that serves to funnel the injected current toward the center of the active region for better fundamental optical mode and gain overlap. While the AR and the TJ have been studied extensively and optimized to improve device performance, the only considerations typically mentioned in the literature for the OA are optimum placement at nodes of the cavity resonance, material grading, tapering, and layer thickness. However, doping of the OA within the microcavity has not been discussed to the best of the author's knowledge. This section discusses how doping the OAs placed inside the microcavity of single- or multiple-stage BC LEDs significantly improves overall device performance by reducing the operating voltage, increasing the light power, and reducing junction heating.

OA layers are routinely doped when they are located within a DBR stack in *p-i-n* junction VCSEL and 1-stage BC VCSEL structures [4, 45]. Generally, in single-cavity multiple-AR BC structures, undoped OAs are located within the mostly undoped (except for the degenerately doped tunnel junction layers) microcavity. The OA layers within the microcavity have been shown to reduce bistability effects due to current spreading between successive active regions [22]. Doping the microcavity OAs generally increases losses due

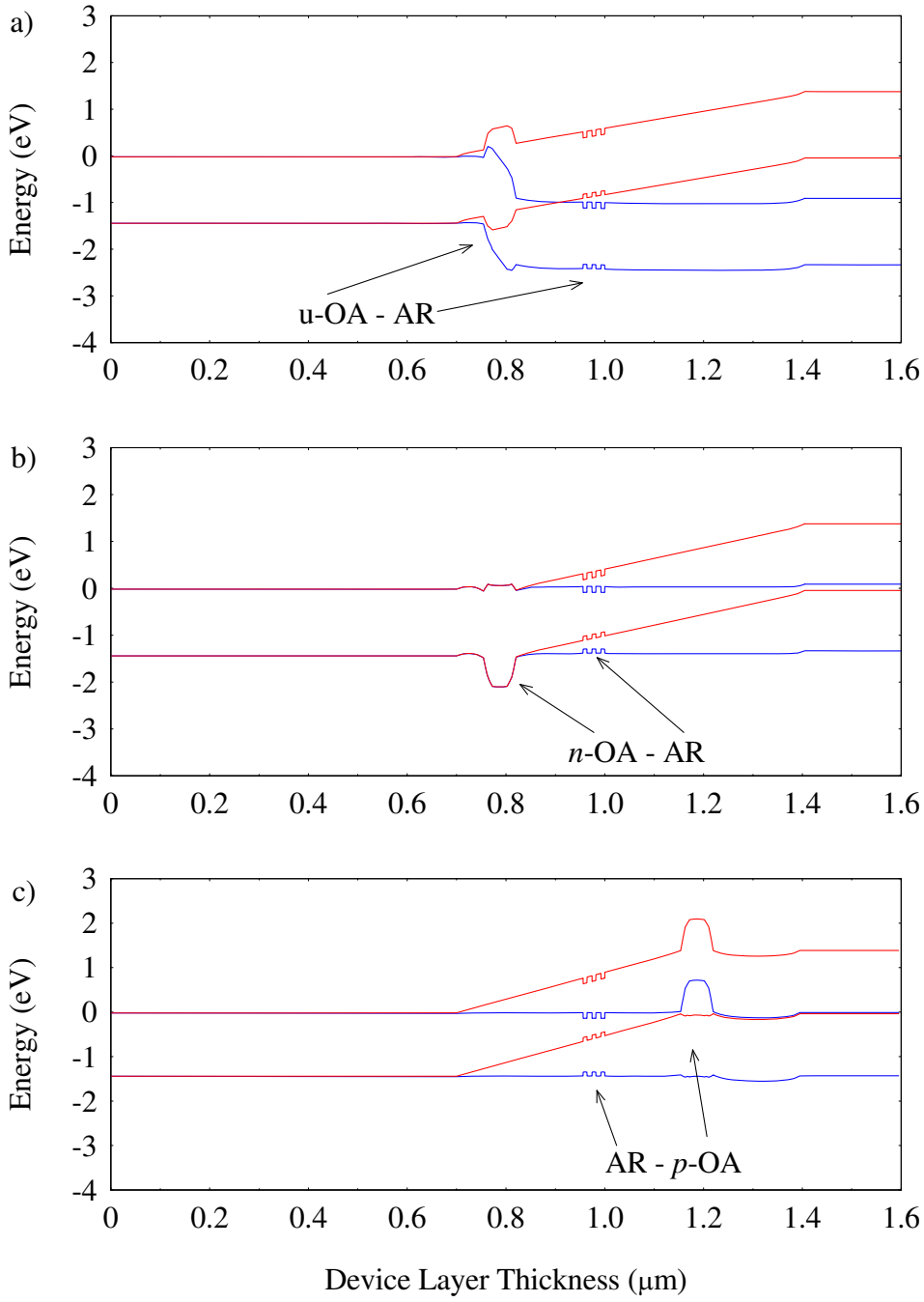


Figure 4.4: Energy band diagrams comparing *p-i-n* LEDs with undoped, n-doped and p-doped OAs. The red energy bands are at 0 V and the blue energy bands are at an injection current of 50 mA.

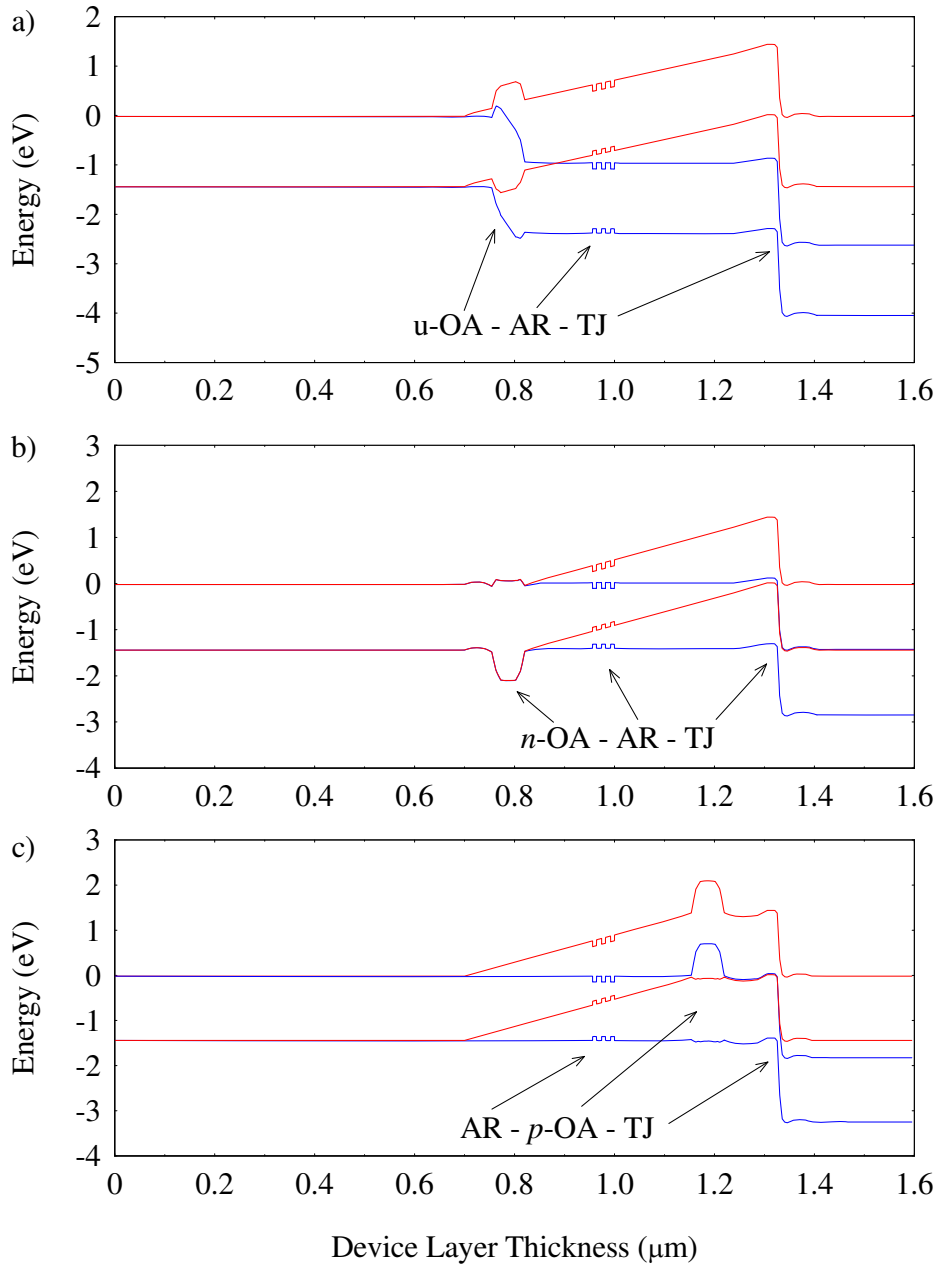


Figure 4.5: Energy band diagrams comparing 1-stage BC LEDs with undoped, n-doped and p-doped OAs. The red energy bands are at 0 V and the blue energy bands are forward biased at an injection current of 50 mA.

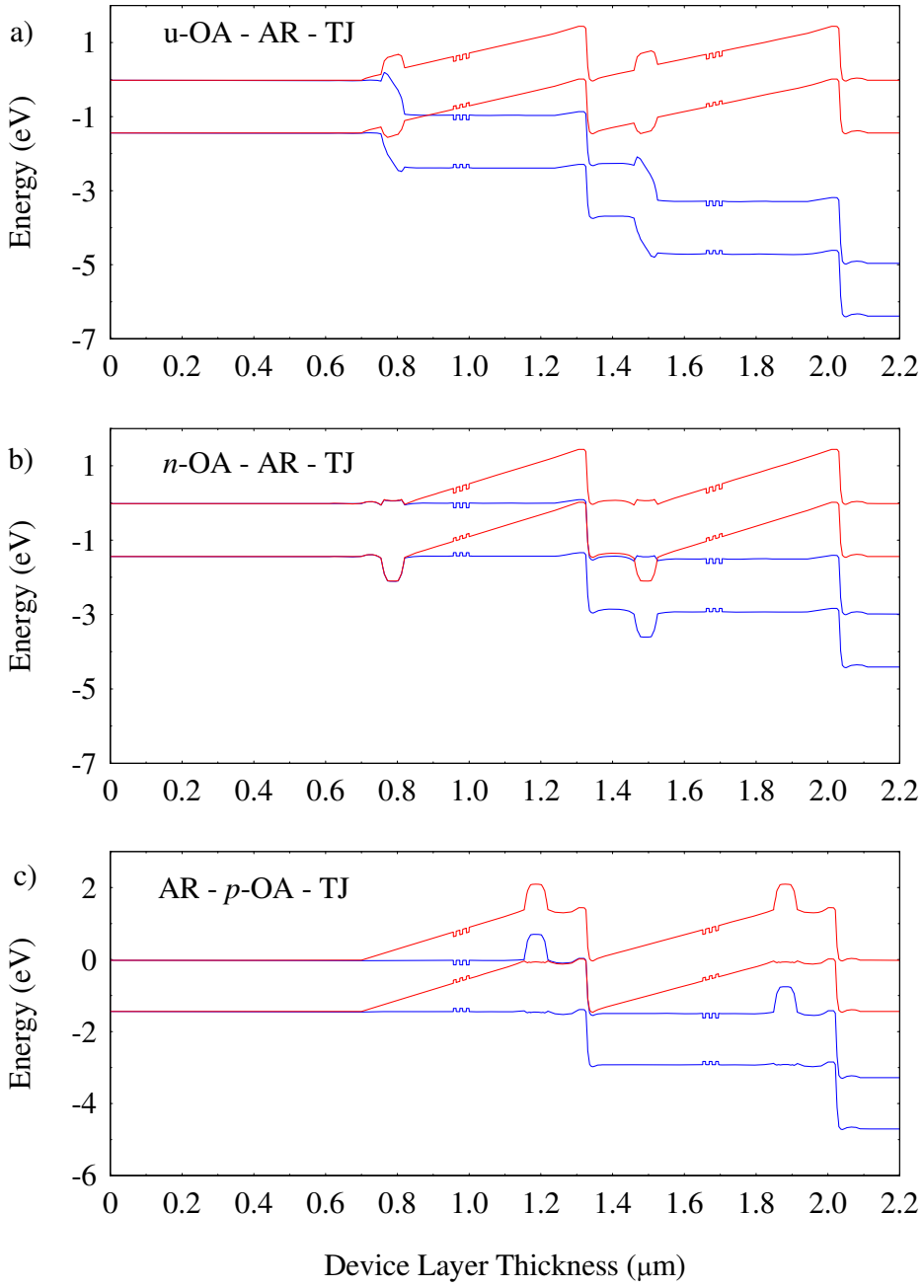


Figure 4.6: Energy band diagrams comparing 2-stage BC LEDs with undoped, n-doped and p-doped OAs. The red energy bands are at 0 V and the blue energy bands are forward biased at an injection current of 50 mA except for the 2-stage p-doped OA BC LED which is at 48 mA. This is due to computational instabilities and software version incompatibilities that did not allow the APSYS software to completely model the 2-stage BC LED across the full 50 mA current range.

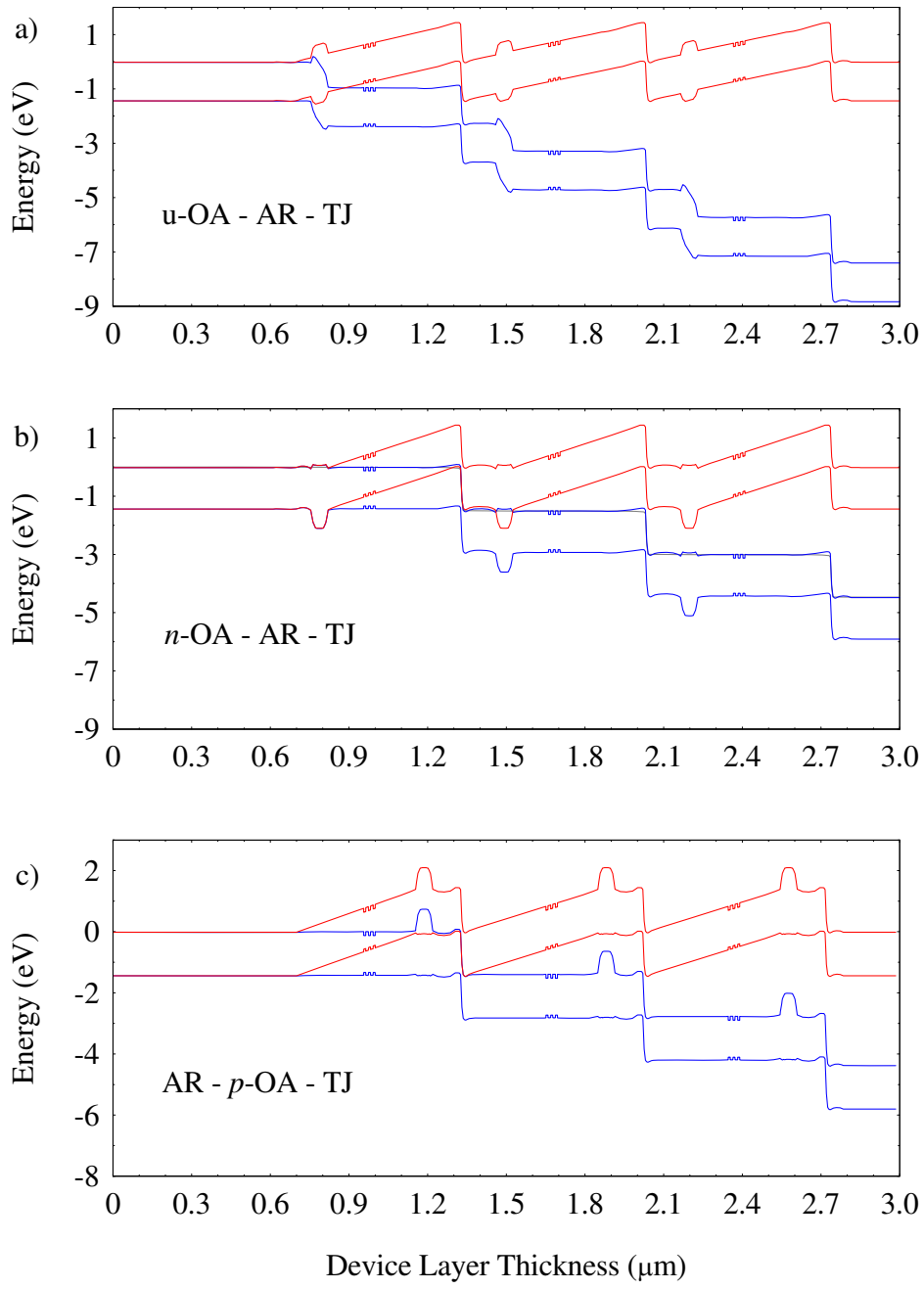


Figure 4.7: Energy band diagrams comparing 3-stage BC LEDs with undoped, n-doped and p-doped OAs. The red energy bands are at 0 V and the blue energy bands are forward biased at an injection current of 50 mA except for the 3-stage p-doped OA BC LED which at a low voltage bias of 4.3 V, which corresponds to less than 1 mA. This low bias is due to computational instabilities and software version incompatibilities that did not allow the APSYS software to completely model the 3-stage BC LED across the full 50 mA current range.

to scattering and free-carrier absorption. However, with proper insertion in the cavity in a resonance node, much of the loss can be avoided. These losses will be shown to be much less than the gains achieved by doping the OAs.

This investigation focuses on the OA layers and the evolution of the experiment designed around a systematic series of BC LED structures, similar to that shown in the lower panel of Figure 4.8. This structure allows the physics of the microcavity in BC devices to be disentangled from the additional complications that result from laser operation in a similar BC VCSEL structure [**?**].

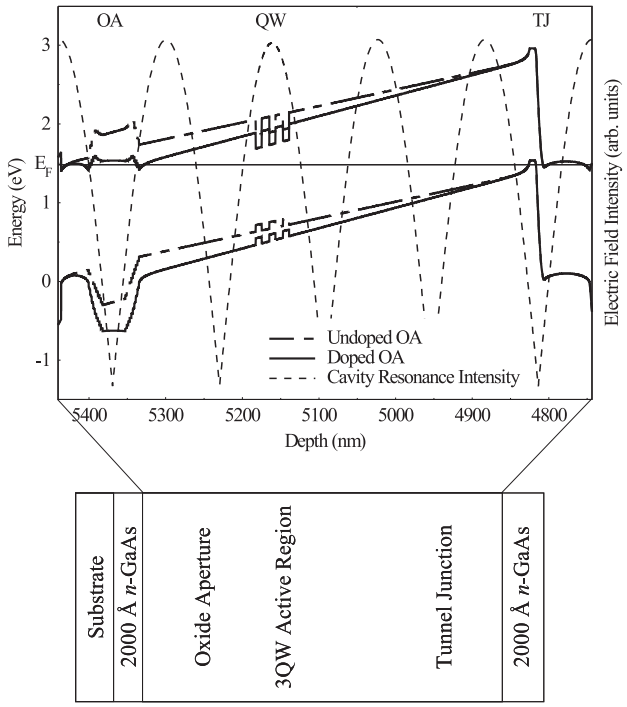


Figure 4.8: Calculated electric-field intensity (dashed lines) and real-space energy band diagrams of a single-stage BC VCSEL with undoped (semi-dashed lines) and doped ($N_d = 2 \times 10^{18}$ cm^{-3}) OAs (solid lines) in and around the microcavity active region (the top and bottom DBRs are not shown). Also shown is a schematic diagram of a single-stage BC LED device with the BC VCSEL microcavity [39].

4.4.2 Bipolar Cascade Light Emitting Diode Growth & Fabrication. To investigate the electrical, optical, and electroluminescent (EL) properties of the microcavities, BC LEDs were grown by MBE in a Varian Gen II system on n-type (100) GaAs substrates consisting of a microcavity designed to be in a $\frac{5}{2}\lambda$ thick *p-i-n* VCSEL or a BC VCSEL struc-

ture with 1-, 2-, or 3-stages. Initially, seven LED (*p-i-n* and BC) structures were grown to quickly evaluate the affects of doping the OA, as well as to determine if thicker TJ layers would be beneficial to BC LED performance. The microcavity is stacked between 2000 Å thick GaAs cladding layers. The *p-i-n* LEDs top cladding layer is C-doped at 4×10^{18} cm^{-3} and the bottom cladding is Si-doped at 4×10^{18} cm^{-3}. The BC LED's cladding layers are both Si-doped at 4×10^{18} cm^{-3}. A 1-stage undoped/n-doped BC LED device is shown schematically at the bottom of Figure 4.8. Each $\frac{5}{2}\lambda$ thick stage consists of a graded OA located in the first node (left to right in Figure 4.8), a triple QW active region located in the third antinode, and a tunnel junction located in the fifth node of the cavity resonance. Placing the OAs and tunnel junctions in the nodes minimizes losses and placing the QW in the antinode maximizes the gain achieved from the cavity. The graded OAs consist of a 180 Å thick $Al_xGa_{1-x}As$ layer with x increasing from 0.1 to 0.9, a 300 Å thick $Al_{0.98}Ga_{0.02}As$ OA (undoped for the *p-i-n*, 1- and 2-stage BC LEDs and n-doped at 2×10^{18} cm^{-3} for the 3-stage BC LED), and a 180 Å thick $Al_xGa_{1-x}As$ layer with x decreasing from 0.9 to 0.1. The AR has three 80 Å thick $In_{0.20}Ga_{0.80}As$ QWs separated by 100 Å thick GaAs barriers. The GaAs TJ consisted of a p^{++} layer C-doped at 5×10^{19} cm^{-3} and an n^{++} layer Si δ-doped with an effective doping level of $\sim 2\times10^{19}$ cm^{-3}. The TJ layers were either 100 Å or 200 Å thick to investigate the minimum layer thickness required for optimal device performance. Additional TJ growth details appear elsewhere [37].

The next series of crystal growth consisted of five samples grown consecutively to fill in the comparison matrix between undoped and n-doped OA BC LEDs. The five samples all had 200 Å thick TJ layers because, as seen in Section 4.4.3, the BC LEDs with 200 Å thick TJ layers significantly outperformed the BC LEDs with 100 Å thick TJ layers with respect to light output. The final series of crystal growth consisted of the p-doped OA BC LEDs. Table 4.1 encapsulates the LEDs developed for this study, detailing the time line of sample growth, if the devices were modeled or grown, what the OA doping level was, and the TJ layer thickness. The last two structures in Table 4.1 were modeled for completeness but never grown because *p-i-n* structures were not necessary because any information obtained would not influence the BC structures.

Although the MBE is constantly being recallibrated to ensure ternary compositions and growth rates are well defined, due to the system complexity changes in the MBE system make it very difficult to keep the uncertainty of the InGaAs composition and growth rate to a minimum. The ternary growth is always "best effort" because for a research effort like this device research would rapidly become cost prohibitive. This makes defining a QW to emit at 980 nm to be an uncertain process. This will be seen in the electroluminescence characterization illustrated in this chapter.

Table 4.1: Modeling and Growth details for *p-i-n* and BC LED structures. The lines separate the growth runs. The first seven samples were grown consecutively, the next four samples were grown at a later date consecutively, and the last three samples were grown consecutively.

Structure	Modeled Y/N	Grown Y/N	OA Doping Concentration (10^{18} cm^{-3})	TJ Layer Thickness (Å)
p-i-n n-doped OA	Y	Y	2	No TJ
1-Stage n-doped OA	N	Y	2	100
1-Stage n-doped OA	Y	Y	2	200
2-Stage n-doped OA	N	Y	2	100
2-Stage n-doped OA	Y	Y	2	200
3-Stage Undoped OA	N	Y	Undoped	100
3-Stage Undoped OA	Y	Y	Undoped	200
3-Stage n-doped OA	Y	Y	2	200
4-Stage n-doped OA	N	Y	2	200
1-Stage Undoped OA	Y	Y	Undoped	200
2-Stage Undoped OA	Y	Y	Undoped	200
1-Stage p-doped OA	Y	Y	2	200
2-Stage p-doped OA	Y	Y	2	200
3-Stage p-doped OA	Y	Y	2	200
p-i-n Undoped OA	Y	N	Undoped	No TJ
p-i-n p-doped OA	Y	N	2	No TJ

The samples were processed into LEDs with square mesas and 5 μm-wide square annulus top metal contacts 5 μm inside the perimeter of the mesa. The top and bottom (backside metal) ohmic contacts consist of a Ni:Ge:Au:Ni:Au metal layer profile that was annealed in forming gas (95% Ar - 5% H_2) at 410 $^\circ$C for 15 seconds. Each device was dry etched using a BCl_3-Cl_2 recipe through the active region to form isolation mesas. The OA

layers were never oxidized because these are BC LEDs and the investigation was to study the effects of doping the AlGaAs OA layer and not the oxidized material.

4.4.3 Bipolar Cascade Light Emitting Diode Characterization. LED characterization consisted of VI, LI, EL, and intensity characterization. Room temperature VI and LI characterization was performed using a Cascade Microtech probe station, an HP 4145A semiconductor parameter analyzer (SPA), and a 1 cm diameter Si *p-i-n* photodetector positioned above the needle probe to maximize light collection across the entire current range. Since the photodetector was above the probe, the collected light values are maximized relative values not absolute values. The EL characterization used the SPA as the constant current source operating at 50 mA; the output light was coupled into a silica multimode fiber (core diameter of 63 μm) aligned to maximize the collected light and measured using an HP 70951B optical spectrum analyzer. Again, the power values are maximized relative values and not absolute values. The intensity characterization used the SPA as the constant current source operating at 50 mA; the LEDs were imaged using a Spiricon 980M near-infrared camera and image capture software. The camera was operated with linear gain and not auto-gain compensation, allowing all images to be compared directly.

Initial characterization, shown in Figure 4.9, indicated significant improvement in both voltage and light performance with n-doped OAs. The 1- and 2-stage devices scaled at nearly 1.5 V. This is slightly higher than a typical 980 nm InGaAs QW LED which has an average operating voltage of 1.2 V. The increase can be attributed to the TJ and OA. However, the 3-stage undoped device scaled at $\sim$2.7 V, caused almost entirely by the undoped OA creating a conduction band electron barrier discussed in Section 4.3. It is also clearly evident that the n-doped OA has a significant effect on the device performance in both the operating voltage, as well as the light output characteristics.

The Figures 4.10, 4.11, and 4.12 present the VI, LI and EL characterization. In all of these figures, the first panel details undoped OAs, the second panel details n-doped OAs, and the third panel details p-doped OAs. The lines are Crosslight APSYS simulation results and the data points (open circles and upsidedown triangles) are measured device

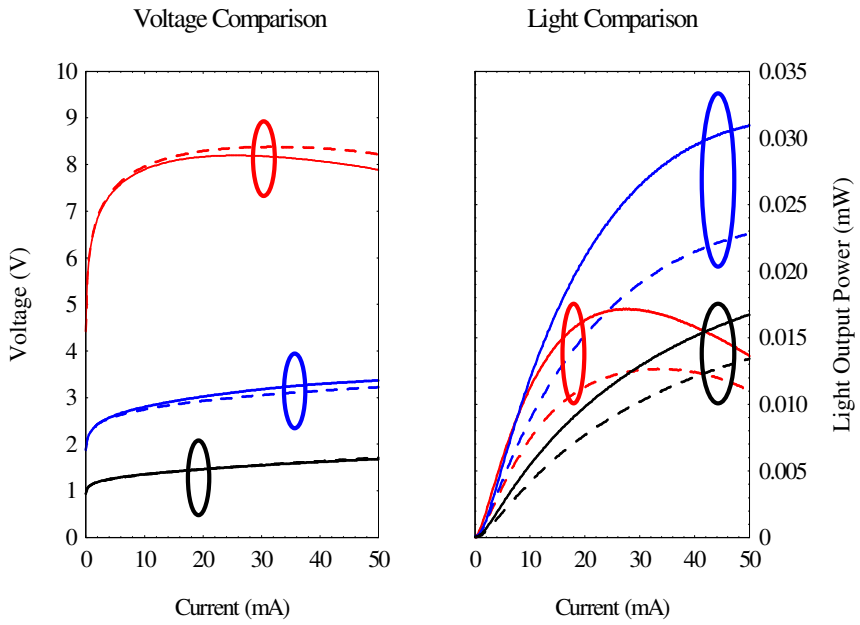


Figure 4.9: Comparison to determine the optimum tunnel junction layer thickness. The black traces are 1-stage BC LEDs; the blue traces are 2-stage BC LEDs; and the red traces are 3-stage BC LEDs. The solid-line traces are devices with 200 Å TJs and the dashed line traces are devices with 100 Å thick TJs. Voltage comparison is inconclusive; however, the light output power comparison clearly indicates the 200 Å thick layer thickness is far superior.

results. The color scheme is the same for all panels, the 1-stage devices are black, the 2-stage devices are blue, the 3-stage devices are red, the 4-stage device is green, and the *p-i-n* device is dashed black with the upsidedown triangles.

Figure 4.10 summarizes the voltage characterization, as well as simulation results for all but one of the structures. The samples all scale in voltage with increased number of stages, as expected, and all agree with simulations. The undoped OA structures deviate the most from simulations. This is believed to be due to more excessive heating in these structures that is not adequately modeled. Significant reductions in operating voltages are clearly observed for the doped-OA devices, compared to the undoped-OA devices. Nearly uniform voltage steps going from one to three BC stages are observed. This indicates that the one to three combinations of OA and TJ are the dominant series resistances, as is expected for good devices. The doped-OA devices demonstrate nearly a 50% reduction

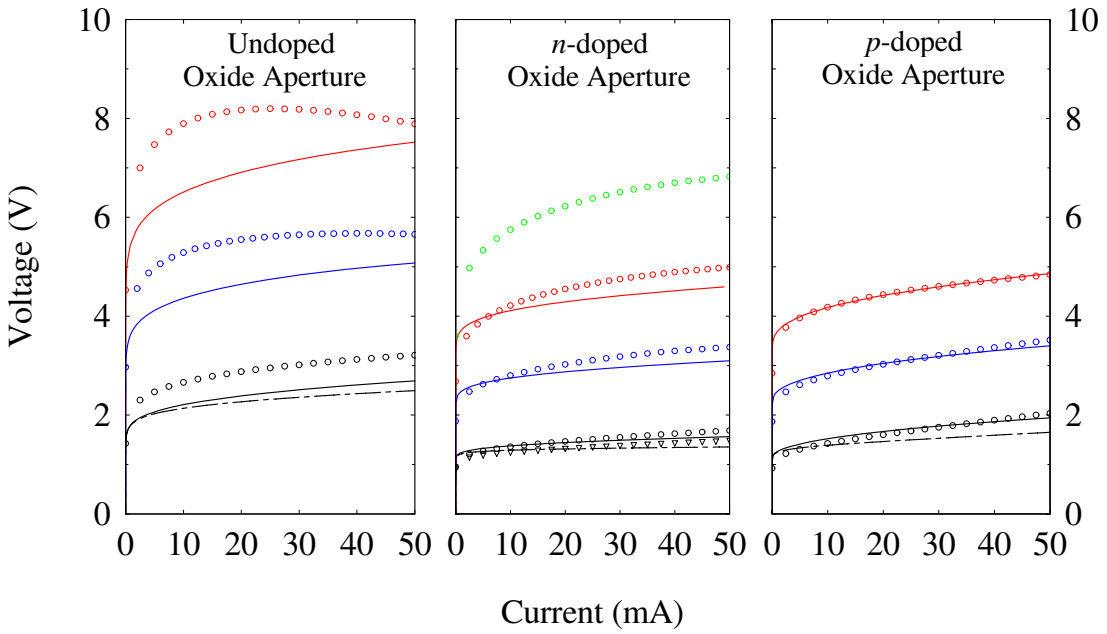


Figure 4.10: Voltage comparisons of standard and BC LEDs. The solid lines are simulation results and the points are measured device results. The color scheme is the same for all panels, the 1-stage devices are black, the 2-stage devices are blue, the 3-stage devices are red, the 4-stage device is green, and the *p*-*i*-*n* device simulation result is a dashed black line and the measured results are upsidedown triangles. The doped and undoped aperture structures all scale with the number of active regions.

in operating voltage when compared to the undoped-OA devices with the same number of stages, and is further corroborated by the simulations. The scaling between successive stages is very uniform, with about 1.5 V per stage for the doped graded OA structures and about 2.7 V per stage for the undoped-OA structures. Significantly, the 3-stage doped OA LEDs have lower operating voltages than the 2-stage undoped OA LED.

Figure 4.11 summarizes the light characterization and indicates the dramatic improvement in output light intensity that is achieved by cascading active regions as well as the improvement by doping the OAs. The undoped OA structures generate much less light as well as show thermal roll off occurring at much lower injection currents. This is evident for all numbers of device stages. The undoped and n-doped OA devices catastrophically failed (by blowing off the metal contacts) more readily, forcing the testing to stop at 50 mA. However, the p-doped devices were significantly more robust and were only limited by the SPA used to test the devices. The 2- and 3-stage devices with n-doped OAs have

a nearly a 160% and 200%, respectively, improvement in light power at 30 mA over the undoped OA devices.

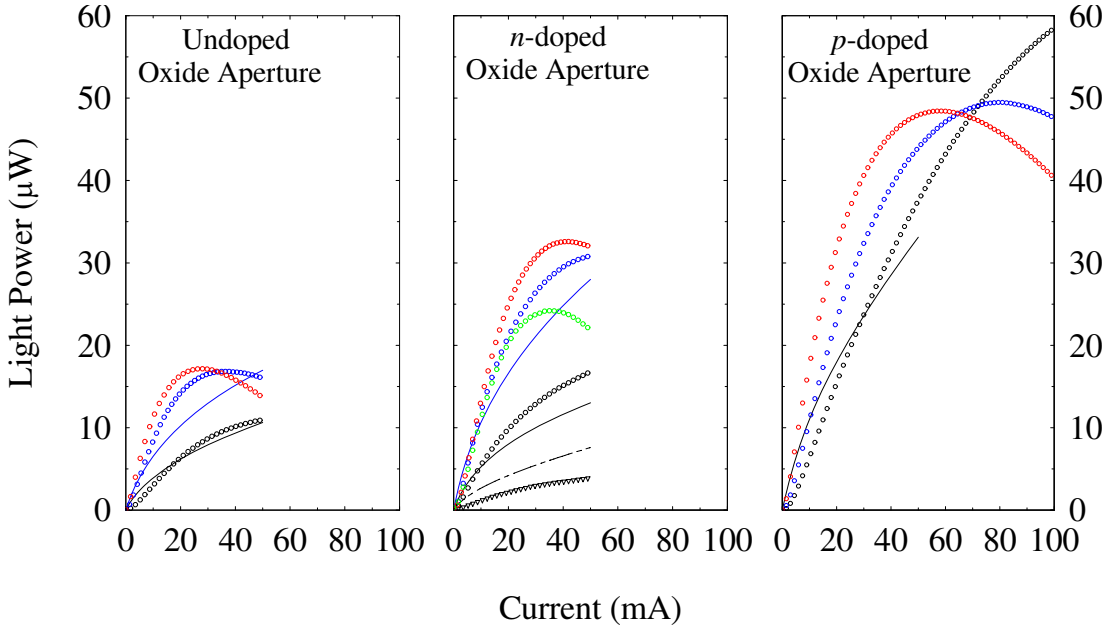


Figure 4.11: Light output comparisons of standard and BC LEDs. The solid lines are simulation results (which were scaled appropriately) and the points are measured device results. The color scheme is the same for all panels, the 1-stage devices are black, the 2-stage devices are blue, the 3-stage devices are red, the 4-stage device is green, and the *p*-*i*-*n* device is black but with upsidedown triangles and a long dashed line. Nearly all the doped OA BC LED devices outperform the undoped OA devices.

Saturation effects are also evident in the devices due to junction heating. The LI curves of the undoped OA devices roll over at smaller current densities due to increased junction heating as a result of the larger electron injection barrier. It is also evident that there is a limit to the number of stages that can be implemented to improve the light output due to junction heating. The output power and overall power conversion efficiency of the 4-stage n-doped BC LED both decreased as compared to the 3-stage n-doped device. Table 4.2 indicates the current where the thermal saturation effects occurs for each device.

The APSYS software simulated results do not appear to predict the thermal saturation effects or light output scaling for multi-stage BC LEDs as well as it does the electrical properties for multi-stage BC LEDs. This may result from the difficulty in computationally

accounting for the increased number of electrons and holes available for optical recombination due to the barriers formed by the doped OAs.

The question arises as to why the 2- and 3-stage p-doped devices do not perform as well as the 1-stage device. Returning to the band diagrams in Figures 4.5-4.7 will provide some insight. For the 1-stage device, the number of conduction band electrons near the QWs is very large and are effectively blocked from traversing the entire length of the device by the OA. Also, the band of tunneling states is large ($\sim$0.75 eV) for valance band electrons to tunnel into the conduction band, generating holes for optical recombination, in the QWs. For multiple-stage devices, the subsequent injection of conduction band electrons is limited by the rate of optical recombination creating valence band electrons, as well as the rate valence band electrons can tunnel into the next stage. The TJs in the stages nearest the substrate exhibit relatively small bands of tunneling states ($<$0.1 eV) with the topmost TJ exhibiting the largest band of tunneling states ($\sim$0.5 eV and $\sim$0.4 eV for the 2- and 3-stage devices, respectively). Presuming the BC LED modeling is correct, it is not clearly understood why only one of the TJs band overlap increases with increased bias and not all of the TJs equally. Further investigation of this may be able to provide significant improvements in p-doped OA BC emitters. One possible avenue of investigation is to include a barrier (either a doped GaAs region or another OA) opposite the QW from the OA.

Figure 4.12 summarizes the EL for the *p-i-n* LED and the 1-, 2-, and 3-stage devices. The undoped OA samples exhibit significantly lower QW luminescence and have pronounced red shifts in the GaAs emissions as compared to the doped OA samples. These differences are attributed to greater device heating in the undoped OA samples. These shifts are tabulated in detail in Table 4.2. The GaAs peak wavelengths indicate larger red shifts per stage for the undoped OA structures ($\sim$13.5 nm) as compared to the doped OA structures ($\sim$7-9 nm). It can be argued that the EL peak will scale linearly with the number of cascaded stages for both doped and undoped OA structures. If the EL peak for the 3-stage doped structure did not suffer from heating effects, the peak would most likely scale such that the emission peak would be linear with EL peaks of the 1- and 2-stage undoped structures. Due to growth uncertainties of the InGaAs QWs the peaks may or may not follow

Table 4.2: Current at thermal rollover, EL peak wavelengths, and EL area analysis at 50 mA for doped and undoped 50 μm $\times$ 50 μm square OA devices at room temperature.

Structure	LI Peak Current (mA)	GaAs Peak (nm)	QW Peak (nm)	EL Area (arb. units)
1-Stage Undoped OA	$\sim$50	874.1	995.4	238
2-Stage Undoped OA	35.6	880.2	992.7	490
3-Stage Undoped OA	26.3	887.6	989.4	534
p-i-n n-doped OA	$>$50	872.0	974.7	78
1-Stage n-doped OA	$\gg$50	872.0	972.7	360
2-Stage n-doped OA	$>$50	874.7	976.0	755
3-Stage n-doped OA	39.4	878.7	987.3	888
4-Stage n-doped OA	34.5	884.7	995.3	707
1-Stage p-doped OA	$\gg$100	872.3	968.4	615
2-Stage p-doped OA	78.6	877.6	969.8	877
3-Stage p-doped OA	57.4	881.6	985.0	1150

the GaAs peaks as well. This is observed in the 3-stage undoped-OA BC LED where one can observe that the InGaAs QW peak has a shorter wavelength as compared to the 1- and 2-stage undoped OA BC LEDs. The best explanation for this is that the 1- and 2-stage undoped OA BC LED material was grown several weeks after the 3-stage undoped OA BC LED and the growth environment has changed enough to add this uncertainty.

Another interesting observation from Figure 4.12 is the appearance that more light is emitted by the n-doped OA BC LEDs than by the p-doped OA BC LEDs, in contrast to the LI results in Figure 4.11. While spectrally this is true at the design wavelength of $\sim$980 nm, the detector used for collecting the light in Figure 4.11 collects the entire waveband of emitted light. Therefore, the total integrated output must be considered for the LI. The final column in Table 4.2 quantifies the area of each EL measurement and corroborates the LI data in Figure 4.11 very well. Then, why does the p-doped OA BC LED have a smaller and flatter peak at the design wavelength? One explanation is that the p-doped OA barrier allows for a larger number of electrons and holes to accumulate in the conduction and valence bands, respectively, thus allowing an increased bulk GaAs optical recombination. There is evidence of this in Figure 4.12; the GaAs peak for all three p-doped OA BC LED samples are appreciably larger than the two other types of BC LEDs. Another explanation

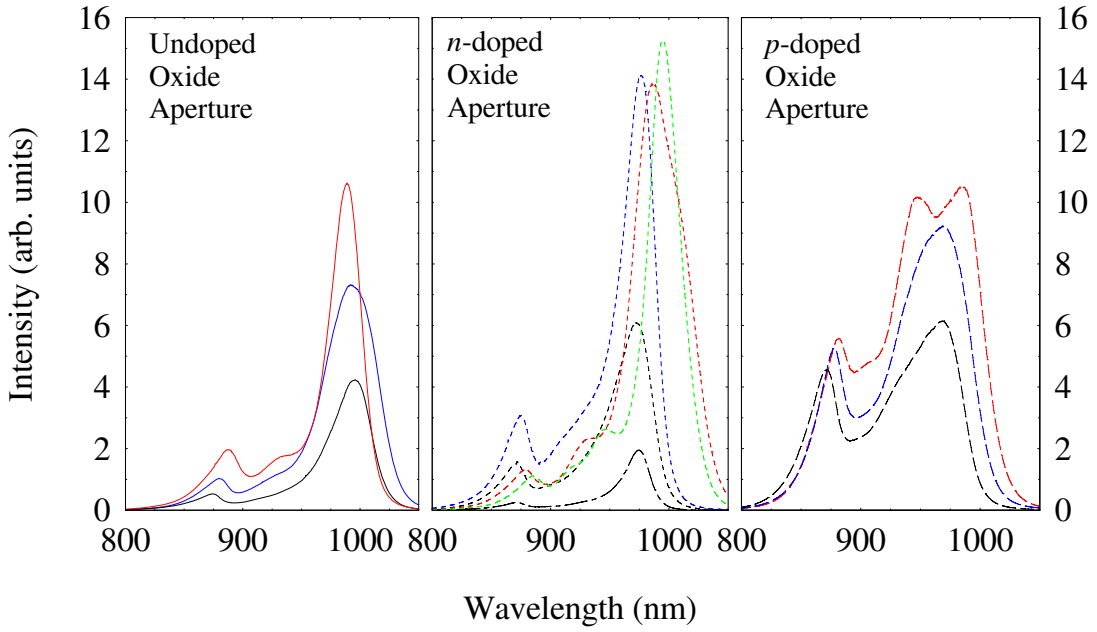


Figure 4.12: Measured EL comparisons of standard and BC LEDs at a current of 25 mA. The color scheme is the same for all panels, the 1-stage devices are black, the 2-stage devices are blue, the 3-stage devices are red, the 4-stage device is green, and the *p*-*i*-*n* device is black with a long dashed line. The doped OA BC LED devices all have stronger QW emission and do not exhibit as significant of a red shift due to device heating as the undoped OA devices.

is the p-doped OA BC LEDs were grown several months after the undoped and n-doped OA BC LEDs and environmental changes in the MBE may have affected the QWs. The broad and, in the case of the 3-stage sample, double peak of the InGaAs signature in the p-doped BC LED relative to the other BC LED InGaAs peaks in Figure 4.12 gives evidence of material growth issues.

Figure 4.13 shows the improvements in luminescence uniformity between a *p*-*i*-*n* LED and a single-stage BC LED with n-doped OAs at an operating current of 50 mA under identical image capture conditions. With the standard *p*-*i*-*n* junction LED, it is evident that the luminescence is limited to the region around the top metal contact, whereas the single-stage BC LED luminescence profile is significantly more uniform. The improvement is due to uniform spreading of the higher mobility electrons across the whole LED mesa in

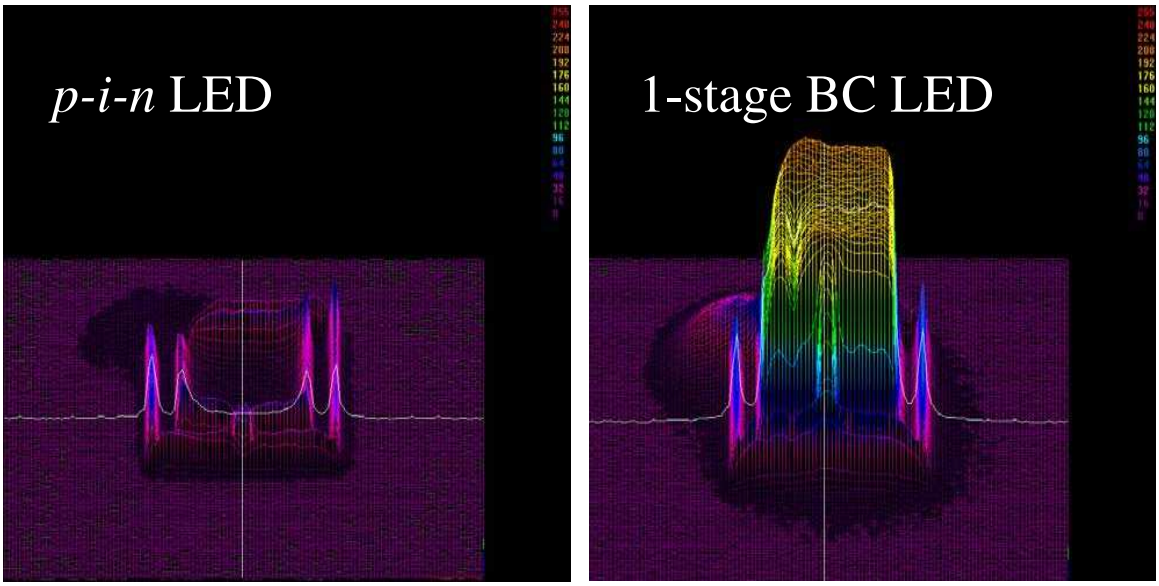


Figure 4.13: Near-field intensity image of a 50 μm $\times$ 50 μm square mesa *p-i-n* LED (left) and a 1-stage BC LED with an n-doped OA layer (right) at a current injection of 50 mA. The camera intensity scale is identical for both devices.

the n-cladding and highly doped n-layer of the TJ then uniformly tunneling to efficiently provide holes into the valence band of the QWs.

Figure 4.14 shows luminescence uniformity for a) the *p-i-n* LED, b) 1-, c) 2-, d) 3-, and e) 4-stage BC LEDs with n-doped OAs at an operating current of 50 mA under identical image capture conditions. In all BC structures the uniformity is very consistent. The 4-stage BC LED shows the reduction of light output due to heating and the large power consumption.

This research shows that doping the graded intracavity OA layers of BC LEDs significantly improves device performance by reducing the required voltage, increasing optical recombination, reducing the red shift due to device heating, and increasing the saturation current where thermal rollover becomes evident. The TJs also improve light output from a given device, primarily by improving the current injection uniformity over the entire aperture of the device.

Clearly, the best choice of design amongst the four LED structures studied (*p-i-n*, undoped OA BC LED, n-doped OA BC LED, and p-doped OA BC LED) is the p-doped OA

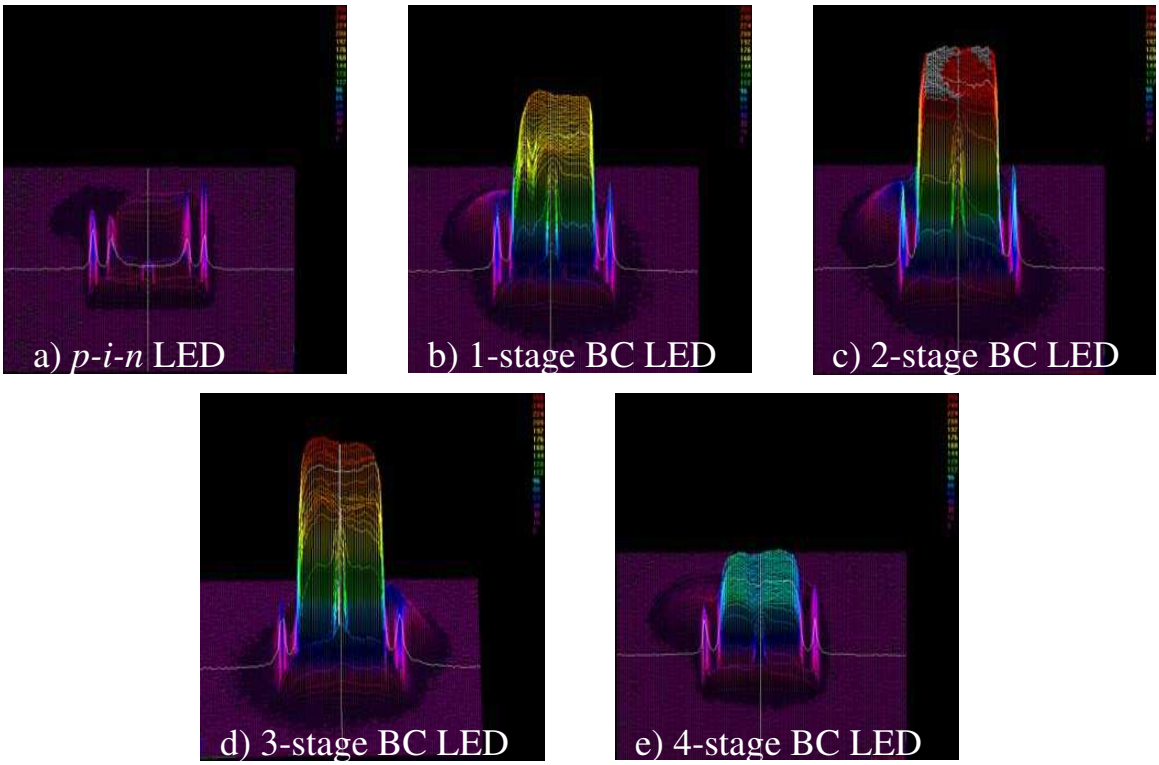


Figure 4.14: Near-field intensity images of 50 μm $\times$ 50 μm square mesa LEDs with n-doped OAs. a) *p-i-n* LED, b) 1-stage BC LED, c) 2-stage BC LED, d) 3-stage BC LED, and e) 4-stage BC LED, operating at a current injection of 50 mA. The camera intensity scale is identical for all devices.

BC LED. Both doped OAs BC LEDs significantly outperform the undoped OA BC LED. However, the p-doped OA BC LED has a significantly larger light output as compared to the n-doped OA BC LED. While the results for the BC LEDs point to the p-doped OA as the best device, this does not take into consideration of the cavity effects when incorporated into a VCSEL structure. Crosslight software capable of modeling the BC VCSEL structures was not able to be purchased due to the significant investment required. Therefore, with the results of the BC LED modeling and experimental data, the p-doped OA structure was chosen as the best structure for incorporation into the BC VCSELs for growth, fabrication, and characterization.

4.5 Bipolar Cascade Vertical Cavity Surface Emitting Lasers

4.5.1 Introduction. BC VCSELs are promising for producing signal gain under high-speed modulation conditions in the RF range [28]. A particular application of interest is that of RF-photonic links. BC VCSELs responsive to GHz injected current modulations can be used as the direct-drive optical signal generation device in such systems, greatly simplifying the component requirements and avoiding the insertion losses associated with external modulators. The central feature of BC devices is the use of reverse-biased TJs to efficiently source electron and hole currents to multiple active regions by recycling the valence band electrons resulting from optical recombination. Benefits of BC designs over typical *p-i-n* diode lasers include greater slope efficiency, and quantum efficiencies that can exceed unity when using multiple stages [20], improved RF impedance matching through increased series resistance [13], and reduced noise figures as a result of uncorrelated carrier recycling among stages [26].

Even though high-frequency performance is crucial, few reports of measured BC laser modulation data exist. Despite significant advances in InP- and GaAs-based BC VCSEL structures and their extensive characterizations [17, 23, 32, 44], to date we have located only the high-frequency analysis reported by Knödl, $et\ al.$ [21] wherein modulated current efficiency factors are extracted from relative intensity noise measurements as a means of high-frequency characterization.

High-frequency measurements of modulated laser light output as a function of RF small-signal injected current for a series of BC VCSELs have been accomplished and reported [36, 38, 40]. The details of the growth and fabrication of GaAs-based BC VCSELs with operating wavelengths ~ 980 nm are presented. Measured BC VCSEL characteristics including LI, VI, and light power vs. drive power (LD), and small-signal laser modulation results approaching 10 GHz as a function of temperature are presented and discussed. For LD characterization, the drive power is defined as the device current multiplied by the applied voltage.

4.5.2 Bipolar Cascade Vertical-Cavity Surface-Emitting Laser Growth & Fabrication. Figure 4.15 a) illustrates the schematic layer diagram for a single-stage BC VCSEL structure, Figure 4.15 b) is a micrograph of a fabricated high-speed BC VCSEL device, and Figure 4.15 c) is a close-up scanning electron microscope (SEM) image of the BC VCSEL aperture. The BC VCSELs were grown on n^+ GaAs substrates by MBE. The laser cavities consist of 1-, 2-, or 3-stage $\frac{5}{2}\lambda$ microcavities, each containing a graded p-doped $Al_{0.98}Ga_{0.02}As$ OA [39] and a GaAs TJ [37] positioned at longitudinal nodes of the optical standing wave, and a triple QW active region placed at an antinode.

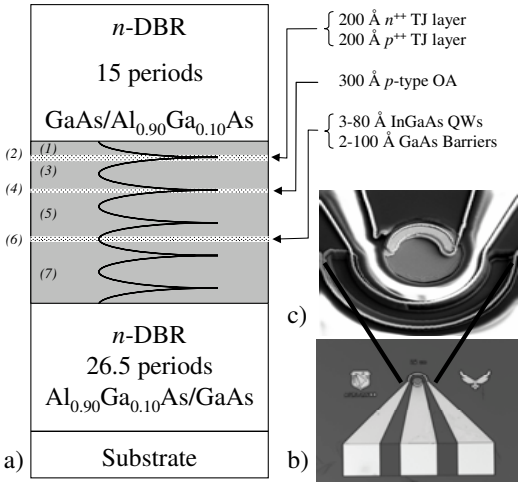


Figure 4.15: a) Schematic layer diagram of a single-stage BC VCSEL. The curve indicates the optical field of the $\frac{5}{2}\lambda$ cavity resonance. The insets show b) a micrograph of a processed high-speed device and c) a close-up SEM image of the VCSEL aperture.

The following description gives the layer structure for a 1-stage device. The top DBR consists of 15 abrupt GaAs/$Al_{0.90}Ga_{0.10}As$ pairs, Si-doped at 4×10^{18} cm^{-3}, each $\frac{\lambda}{4}$ thick. The microcavity is formed from the top DBR as follows (numbering scheme is indicated in Figure 4.15 a). First, an undoped GaAs spacer layer *(1)* is used to center a TJ *(2)* at the first node. The TJ is composed of a Si δ-doped GaAs layer with an effective doping level of 2×10^{19} cm^{-3} and a C-doped GaAs layer (doped at 1×10^{20} cm^{-3}); each TJ layer is 200 Å thick. Below this, an undoped GaAs spacer layer *(3)* positions an OA region *(4)* at the next node of the standing wave. The 300 Å thick OA is p-type $Al_{0.98}Ga_{0.02}As$ and has graded transition layers on either side. Under the OA is an approximately $\frac{3}{4}\lambda$ thick undoped GaAs

spacer layer *(5)* designed to place the active region in an antinode. The active region *(6)* consists of three 80 Å thick $In_{0.20}Ga_{0.80}As$ wells separated by 100 Å thick GaAs barriers. Finally, an undoped GaAs layer *(7)* approximately 1-λ thick is used to complete the cavity. For 2- and 3-stage structures, the entire microcavity is repeated. The bottom DBR consists of 26.5 abrupt $Al_{0.90}Ga_{0.10}As$/GaAs pairs with the same layer thicknesses and doping as the top DBR.

Top-contacted, mesa-isolated BC VCSELs with circular mesas varying from 10 to 50 μm in diameter were fabricated. Appendix B details the fabrication process. Semi-ring annuli ohmic top contacts were formed lithographically and contact metal (50 Å Ni / 170 Å Ge / 330 Å Au / 150 Å Ni / 3,000 Å Au) was evaporated onto the patterned topside. The mesa dry etch was stopped on the third GaAs layer of the bottom DBR, just below the cavity as determined by in-situ reflectivity. The bottom contact was patterned and the same metals were deposited on both the patterned side and the backside (for thermal contact). The contacts were annealed in forming gas at 410 °C for 15 s. This annealing step was performed to allow for preoxidation device characterization. The OAs were formed with an in-situ oxidation furnace [11] at 400 °C for four hours, yielding an approximate 10 μm oxide penetration depth. The anneal and subsequent oxidation did not affect the quality of the ohmic contacts. Next, a 5,000 Å thick Si_3N_4 layer was deposited for electrical isolation and sidewall passivation, followed by a 5 μm layer of SU-8 (a very thick epoxy-based negative photoresist) used for planarization. The mesas and bottom contacts were opened lithographically and the uncovered Si_3N_4 was subsequently dry etched with Freon 23-O_2 (40 sccm-2 sccm) to completely clear out the mesa aperture and the electrical contacts. The ground-signal-ground *(g-s-g)* cascade contact pads were lithographically defined and Ti - Au (200 Å - 4,000 Å) layers were sputter deposited to ensure step coverage.

4.5.3 Bipolar Cascade Vertical-Cavity Surface-Emitting Laser Characterization.

The BC VCSELs were characterized to determine standard operating characteristics, as well as their high-speed performance. CW LI, VI and LD characteristics for 1-, 2-, and 3-stage BC VCSEL devices were measured at temperatures of -50 °C, -25 °C, 0 °C, and

+25 °C. The BC VCSEL characterization used the same system as for the BC LED characterization, discussed in Section 4.4.3, except a 5% neutral density (ND) filter was included to keep from saturating the photodetector.

Pulsed LI, LD, and VI characterization was not able to be performed on the BC VCSELs. While the AFRL Sensors Directorate has pulsed laser characterization capability for edge emitting lasers, the detector head cannot fit into the probe station's environmental chamber. Pulsed laser characterization would have provided valuable laser operating characteristics while neglecting the CW heating effects.

Table 4.3 details the complete characterization matrix for all temperatures, device mesa sizes, and number of stages. Laser characterization data was collected if the device lased, indicated by an "L" in Table 4.3, otherwise no data was collected and those devices were ignored for the remainder of the research. Frequency response measurements, indicated by an "F" in Table 4.3, were performed on lasing devices with mesa diameters up to 40 μm in diameter. The larger devices were ignored because of significant multimode operation. For smaller devices, frequency response measurements were not acquired either due to device failure while operating at a constant bias during the measurement or the frequency response was insignificant, $i.e.$, less than 2.5 GHz with a steady -20 dB per decade decay rate.

Analysis of the BC VCSELs was performed as a function of number of stages and as a function of temperature. The complete data analysis appears as a function of stage in Appendix C and as a function of temperature in Appendix D.

High-frequency laser modulation response measurements were performed at the same temperature at 1 or 0.5 mA intervals along the positive slope of the LI curves. The output modulation was determined using the s-parameters obtained from an HP-8720A microwave network analyzer (MNA) [41]. The test system consists of a stable CW current source connected to the Port-1 bias-tee of the MNA. The MNA applies a -10 dBm (0.1 mW) small-signal modulation onto the laser bias. The signal was supplied to the VCSEL by a 40 GHz coaxial microwave cable connected to the microprobe. The modulated light output was

Table 4.3: Complete BC VCSEL characterization matrix. Collected laser characterization is indicated by an L and collected frequency response characterization is indicated by an F.

T (°C)	Mesa (μm)	1-Stage	2-Stage	3-stage
-50	20	L F		
	22	L F	L	L
	24	L F	L F	L F
	26	L F	L F	L F
	28	L	L F	L F
	30		L F	L F
	35		L F	L F
	40		L F	L F
	45		L	L
	50		L	L
-25	20	L	L	
	22		L	L
	24		L F	L F
	26		L F	L F
	28		L F	L F
	30		L F	L F
	35		L F	L F
	40		L	L F
	45			L
	50			L
00	22		L	L
	24		L F	L F
	26		L F	L F
	28		L F	L F
	30		L	L F
	35			L F
	40			L F
	45			L
+25	22			L
	24			L F
	26			L F
	28			L F
	30			L

collected using a 63 μm core multimode fiber and detected using a 25 GHz high-speed detector. The output signal from the detector was returned to port 2 of the MNA via a 40 GHz

microwave cable. The s_{21} and s_{11} parameters were measured by the MNA which was 2-port calibrated from 0.15 GHz to 20 GHz in 0.05 GHz steps and averaged ten times.

In order to compare independent measurements to a common -3 dB standard, the measured and fit frequency responses have been scaled by plotting

$$Response = 20log\frac{|s_{21}| \; or \; |MTF(\omega)|}{|MTF(0)|} \tag{4.1}$$

where MTF is the two-pole modulation transfer function. The two-pole form takes into consideration the low-frequency parasitic peak that was often observed. The scaling has been changed from 10log, as in reference [36], to 20log because the power was measured instead of the field resulting in the square term coming out of the logarithm. This kept the measured -3 dB frequency response at or below the calculated maximum frequency response extracted by the K-factor, to be described later in this section. Unfortunately, the maximum -3 dB frequency response was reduced from 9.3 GHz to 7.1 GHz for the best performing devices.

The functional form for the two-pole MTF fitting function was derived to be

$$|MTF(\omega)| = \sqrt{\frac{A+B+C}{(1+\tau_{par}^2\omega^2)[\gamma^2\omega^2 + (\omega^2-\omega_r^2)^2]}} \tag{4.2}$$

where the independent variable ω is the angular frequency and

$$A = C_m^2(1+\tau_{par}^2\omega^2)\omega_r^4 \tag{4.3}$$

$$B = 2C_mC_{par}\omega_r^2[(\gamma\tau_{par}-1)\omega^2 + \omega_r^2] \tag{4.4}$$

$$C = C_{par}^2[\gamma^2\omega^2 + (\omega^2-\omega_r^2)^2]. \tag{4.5}$$

The fit parameters include: $\omega_r = 2\pi f_r$, the relaxation oscillation frequency; γ, the damping rate; C_m, the single pole MTF amplitude constant; C_{par}, the parasitic amplitude con-

stant; and τ_{par}, the parasitic time constant which is converted to a parasitic frequency, f_{par} by

$$f_{par} = \frac{1}{\tau_{par}}. \tag{4.6}$$

With these fit parameters, other important parameters [7] such as the peak frequency, f_{peak},

$$f_{peak} = \sqrt{f_r^2 - \frac{\gamma^2}{8\pi^2}} \tag{4.7}$$

and the calculated -3 dB frequency, $f_{-3\ dB\ Calc}$,

$$f_{-3\ dB\ Calc} = f_{peak}^2 + \sqrt{f_{peak}^4 + f_r^4} \tag{4.8}$$

are determined. These fitted and calculated parameters were obtained for all frequency response measurements as a function of bias current.

The damping rate is proportional to the square of the relaxation oscillation frequency [3, 5, 7, 19]

$$\gamma = K f_r^2 + \frac{1}{\chi \tau_n} \tag{4.9}$$

where τ_n is the differential carrier lifetime and χ is a factor accounting for carrier transport effects. This K-factor is used to estimate the maximum intrinsic modulation bandwidth when only considering the damping rate by [3, 5, 7, 19]

$$f_{-3dB\ damp} = \frac{2\sqrt{2}\pi}{K}. \tag{4.10}$$

Similarly, the thermally-limited modulation bandwidth is given by [3, 19]

$$f_{-3dB\ therm} = \sqrt{1+\sqrt{2}} f_{r\ max} \tag{4.11}$$

and the modulation bandwidth limited by parasitics is [3, 19]

$$f_{-3dB\ par} = (2+\sqrt{3}) f_{par}. \tag{4.12}$$

Figure 4.16 shows a representative set of measured and fit frequency response data for the 28 μm mesa device at a mount temperature of -50 °C. The frequency response for this device was performed with 1 mA steps from 2 to 12 mA. Figure 4.16 shows current steps from 2 to 6 mA to illustrate the frequency response with respect to injected current.

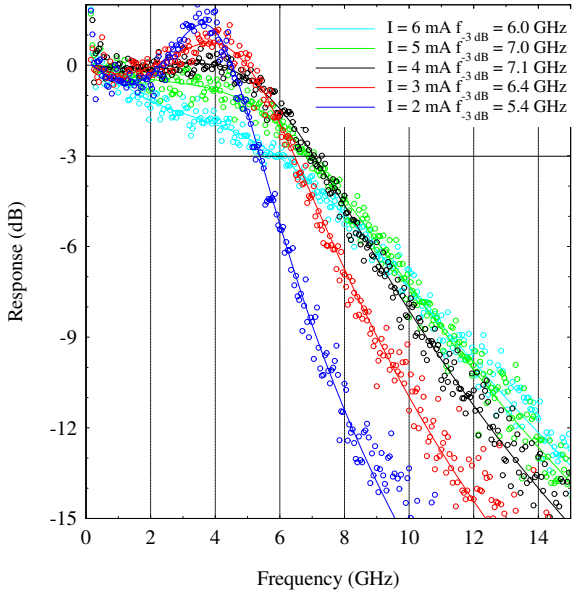


Figure 4.16: Measured and fit frequency responses for 28 μm diameter mesa 3-stage BC VCSELs at a mount temperature of -50 °C. Current steps of 1 mA were performed from 2 mA to 12 mA, but only the 2 through 6 mA data and fits are shown to detail the relation as a function of CW drive current.

4.5.3.1 Standard Laser Characterization Results (LI, LD, and VI). Figure 4.17 shows the operating characteristics for 1-, 2-, and 3-stage BC VCSELs with 28 μm mesas at a chuck temperature of -50 °C. The operating characteristics include CW a) LI, b) LD, c) VI, and d) frequency response characteristics. This mesa and temperature combina-

tion represents the overall best performing single-mode light power and frequency response for both the 2- and 3-stage BC VCSELs. The 1-stage devices lased at -50 °C but not at other temperatures due to low gain resulting from cavity detuning relative to the gain peak and from small round-trip gain due to the low number of DBR pairs and only three QWs. This detuning results in degraded CW performance of all of the BC VCSELs at higher temperatures. The VI data in Figure 4.17 c) unequivocally shows the expected BC VCSEL behavior as the number of stages is increased.

Several mesa diameters lased at all of the temperatures of characterization for the 3-stage BC VCSEL. The best operation in all cases was at -50 °C, but mesas ranging from 22 μm to 30 μm in diameter also lased at room temperature. The most complete set of data occurred for the 3-stage BC VCSEL with mesa diameter of 28 μm, where a complete set of LI, LD, VI, and frequency response characteristics was made over all of the temperatures listed.

The "electron recycling" benefit of the BC VCSEL structure is immediately obvious by comparing the 2- and 3-stage LI and LD data in Figures 4.17 a) and b). The increased round trip gain from the additional stage manifests in a rise in slope efficiency, η_{slope}, from 0.36 W/A for the 2-stage device to 0.46 W/A for the 3-stage device, as well as the reduction in the threshold current from 2.0 mA for the 2-stage device to 0.7 mA for the 3-stage device. Again, the 1-stage LI and LD results are significantly reduced, because of the reasons stated above, with a slope efficiency of 0.05 W/A and a threshold current of 8.0 mA.

An important observation is seen in Figure 4.17 b). It has been repeatedly emphasized in the literature that BC structures do not make light for free. As the number of stages is increased, there will be a corresponding increase in voltage. However, increasing the number of stages reduces the threshold and operating currents and, for the same drive power, the same amount or, as seen in most samples in Appendix C, more light power is generated with additional stages. BC VCSELs improve slope efficiency and improves wall-plug efficiency, $\eta_{wallplug}$!

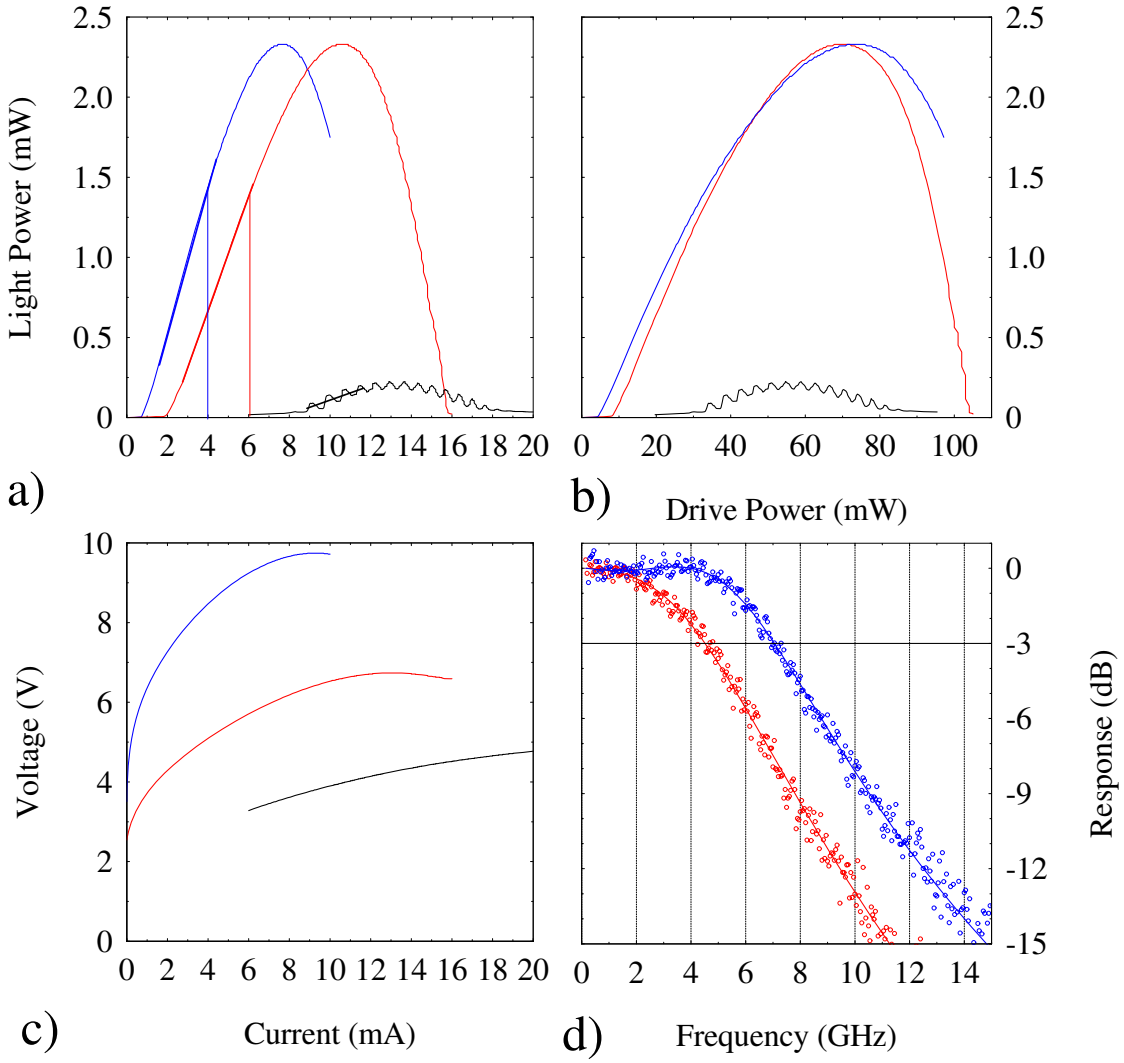


Figure 4.17: Operating characteristics for 28 μm mesa 1- (black), 2- (red), and 3-stage (blue) BC VCSELs at a mount temperature of -50 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The heavy line portions of the LI curves indicate the linear regime where the slope efficiencies were calculated. The vertical lines in a) are the currents where the frequency response characterization was obtained.

As mentioned previously, the 1-stage BC VCSEL did not perform nearly as well as the 2- and 3-stage BC VCSELs due to the low number of DBR mirror pairs reducing the round trip gain in a 1-stage device, thereby requiring the device to be driven harder to achieve threshold and developing undesired heating effects. These heating effects are responsible for the “ripple effect” observed in the LI, Figure 4.17 a), and LD, Figure 4.17 b), characterization [7]. The low-current truncation in the 1-stage LI, LD, and VI is due to

the limited data range of the HP-7145A SPA. A maximum of 256 data steps was available, limiting the current step size or current range. Several devices had this problem, where truncation was required to scan the full lasing range with a current step size small enough to avoid destroying the device being tested.

Figure 4.18 shows the operating characteristics for the 3-stage BC VCSEL with a 28 μm mesa at chuck temperatures of -50 °C, -25 °C, 0 °C, and 25 °C. The operating characteristics include CW a) LI, b) LD, c) VI, and d) frequency response. One can observe that the light power drops off by nearly an order of magnitude from -50 °C to 25 °C. Another observation is the nearly linear translation of the light peak power with increasing drive current, Figure 4.18 a) or power, Figure 4.18 b). This is the key indicator that the InGaAs QW gain peak is poorly aligned with the cavity resonance for room temperature operation. By judiciously reducing the well width, the alignment of the QW gain peak and cavity resonance can be optimized for room temperature operation. Figure 4.18 c) also shows the expected reduction in voltage with increasing temperature due to bandgap narrowing as the temperature increases.

Table 4.4 summarizes several important parameters for these 28 μm devices, including threshold current (I_{th}), slope efficiency (η_{slope}), wall-plug efficiency, ($\eta_{wallplug}$), frequency response drive current ($I_{freq\ resp}$), and -3 dB frequency ($f_{-3\ dB\ Meas}$).

Table 4.4: 28 μm diameter mesa BC VCSEL operating parameters.

Temp. °C	Stage	I_{th} (mA)	η_{slope} (W/A)	$\eta_{wallplug}$ (W_{opt}/W_{elec})	$I_{freq\ resp}$ (mA)	$f_{-3\ dB\ Meas}$ (GHz)
-50	3	0.7	0.46	0.05	4.0	7.1
	2	2.0	0.36	0.05	6.0	4.5
	1	8.0	0.05	0.01		
-25	3	0.7	0.39	0.05	4.0	6.5
	2	1.8	0.28	0.05	4.5	4.3
00	3	0.9	0.32	0.04	3.0	5.3
	2	3.0	0.10	0.02	5.0	2.2
+25	3	1.8	0.13	0.02	3.5	3.4

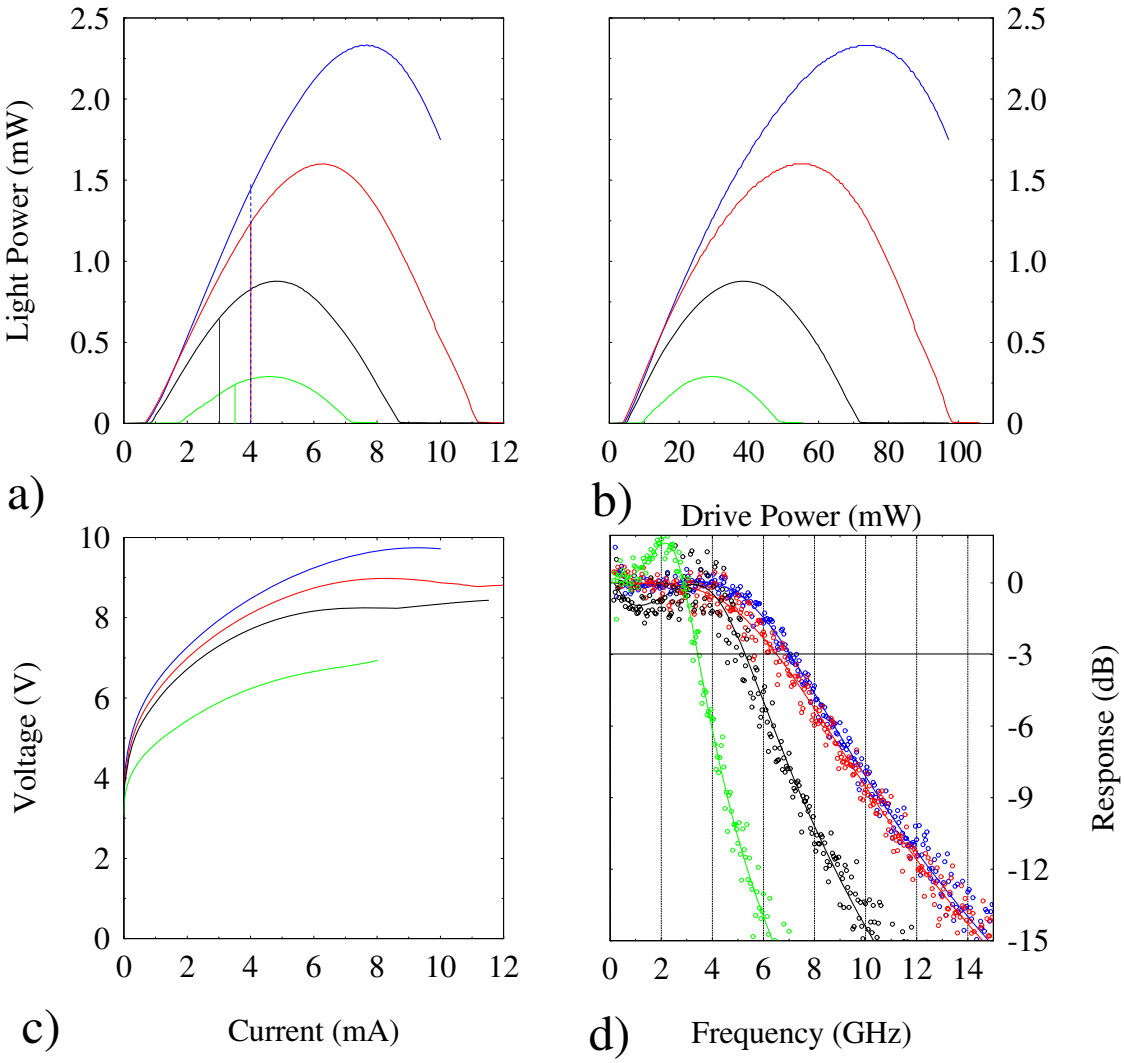


Figure 4.18: Operating characteristics for 28 μm diameter mesa 3-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), 00 °C (black), and +25 °C (green). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

4.5.3.2 High-Speed Laser Characterization Results. Figure 4.17 d) shows the frequency response for the 3- and 2-stage 28 μm diameter mesa devices at the chuck temperature of -50 °C/ [36]. These are the first reported results for BC VCSELs. The 3- and 2-stage BC VCSEL devices exhibit -3 dB frequency responses of 7.1 GHz and 4.5 GHz, respectively, at the labeled biasing conditions. The 3-stage device at +25 °C, shown in Figure 4.18 d), does operate under small-signal modulation with a 3.4 GHz -3 dB response

cutoff. However, the modulation peak is quite sharp, indicating increasing the current injection should increase the -3 dB frequency bandwidth. Unfortunately, the modulation signal falls off at higher bias currents because the laser is operating near the maximum of its positive LI slope, $i.e$ the gain peak is red-shifting out of the cavity resonance. Increasing the current reduces the -3 dB frequency response as the laser operation begins to degrade due to heating effects and increasing gain-cavity mismatch.

The MTF curves for the devices in Figure 4.17 d) correspond to fits with relaxation oscillation frequencies of, $f_r \equiv \omega_r/2\pi =$, 4.78 and 6.27 GHz, and damping rates of, $\gamma =$, 35.4 and 46.3 ns^{-1} for the 2-stage and 3-stage measurements, respectively. Figures 4.19 a) and b) show the damping rate, γ, as a function of resonance frequency squared, f_r^2 for the 3- and 2-stage BC VCSELs, respectively, with 28 μm diameter mesas, as well as the associated K-factor. Figures 4.19 c) and d) show the calculated -3 db frequency, measured -3 db frequency, relaxation oscillation frequency, and peak frequency as a function of $(I - I_{th})^{1/2}$ for the same 3- and 2-stage BC VCSELs, respectively. It is apparent that thermal saturation is an issue with these devices. The roll-off of the peak frequency, f_{peak}, indicates a strong thermal limit to the frequency response along with the strong damping limitation. Parasitic limitations do not appear to be an issue, indicating device design improvements such as (1) improving the room-temperature resonant cavity-InGaAs QW gain peak alignment and (2) grading the DBR mirrors will significantly improve device performance by improving the thermal characteristics of the devices.

Table 4.5 summarizes the high-speed parameters for the 3- and 2-stage BC VCSELs studied in detail and includes a comparison to a SOA room temperature operating 840 nm VCSEL with a 6 μm OA [3]. Since this is the first reported frequency modulation of BC VCSELs there are no BC VCSEL values to compare with. However, a useful comparison with a SOA high-speed semiconductor laser will provide a useful comparison. The K-factor for the BC VCSELs is extremely large (more than $3\times$) compared to the 840 nm VCSEL. This is the primary parameter that must be reduced because it leads directly to a large $f_{-3dBdamp}$ and $f_{-3dbtherm}$.

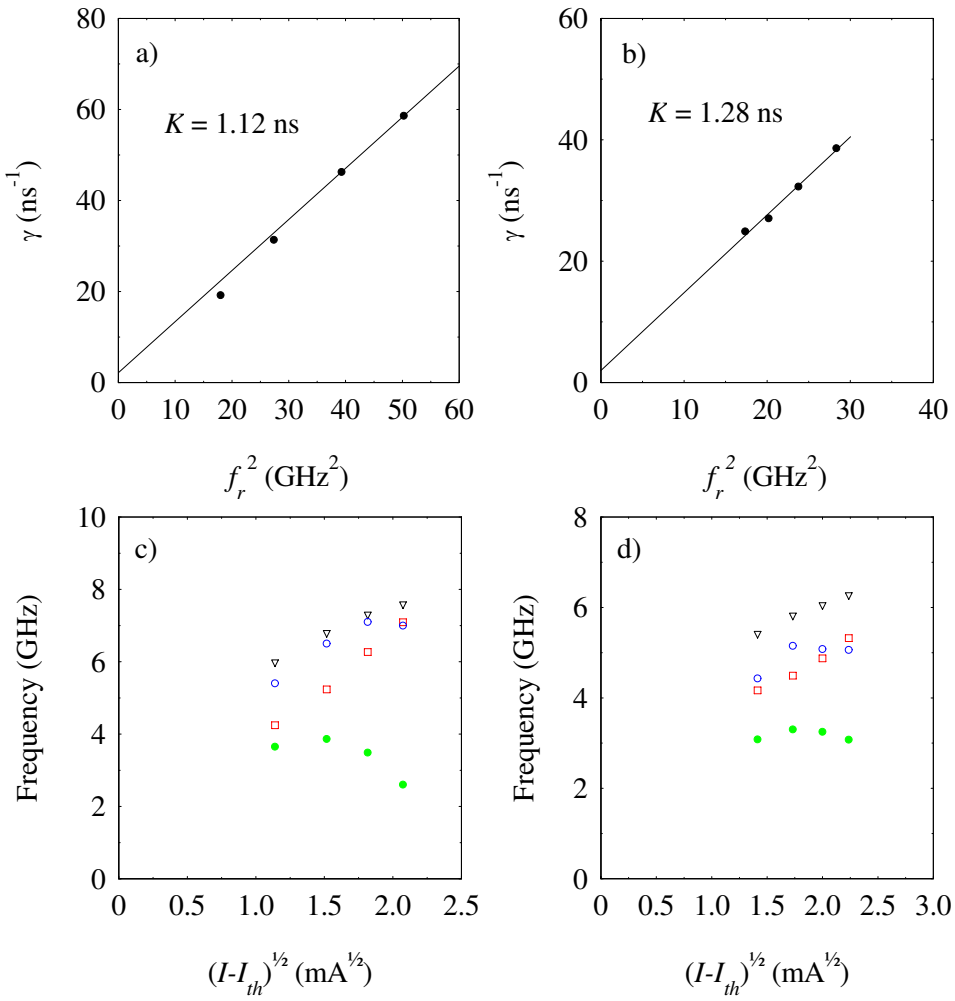


Figure 4.19: High-frequency parameter analysis for 2- and 3-stage BC VCSELs at a mount temperature of -50 °C. a) and b) shows the damping rate, γ, as a function of resonance frequency squared, f_r^2 for the 3- and 2-stage, respectively, BC VCSELs with 28 μm diameter mesas as well as the associated K factor. c) and d) shows the calculated -3 db frequency (black triangles), measured -3 db frequency (blue circles), fitted relaxation oscillation frequency (red squares) and calculated peak frequency (green dot) as a function of $(I - I_{th})^{1/2}$ for the same 3- and 2-stage, respectively, BC VCSELs.

Table 4.5: Frequency modulation parameters for 3- and 2-stage BC VCSELs with 28 μm diameter mesas at -50 °C and a comparison to a state-of-the-art 840 nm VCSEL with a 6 μm aperture operating at room temperature [3].

Parameter	Units	3-Stage BC VCSEL	2-Stage BC VCSEL	840 nm VCSEL
I_{bias}	mA	4	6	4
f_r	GHz	6.27	4.88	9.5
γ	ns^{-1}	46.3	35.4	$\sim$45
$f_{-3\ dB\ Calc}$	GHz	7.30	6.05	8.3
$f_{-3\ dB\ Meas}$	GHz	7.10	5.08	$\sim$8
f_{peak}	GHz	3.49	3.25	6.5
f_{par}	GHz	5.14	8.08	n/a
K	ns	1.12	1.28	0.40
$f_{r\ max}$	GHz	7.10	5.33	9.5
$f_{-3\ dB\ damp}$	GHz	7.93	6.94	22
$f_{-3\ dB\ therm}$	GHz	11.0	8.28	14.7
$f_{-3\ dB\ par}$	GHz	19.2	30.2	24

4.6 Summary

The design and demonstration of 1-, 2-, and 3-stage BC LEDs and VCSELs has been accomplished. The BC LEDs provided unique information on the best layer structure to use in the microcavity of a BC VCSEL. The BC VCSELs all operated at -50 °C and exhibited the first reported frequency response characterization for and type of BCL. The 3-stage BC VCSEL did operate at room temperature. These results show that a BC VCSEL will operate at high-speeds and with high slope efficiencies which are required for an RF photonic link. However, further improvements are required to optimize the BC VCSEL for room temperature operation. First and foremost, the QW gain peak and the cavity resonance has to be better aligned. Other improvements for increasing high-speed operation include DBR mirror pair optimization for the stage to be studied and specially designed fabrication masks to minimize capacitance issues between mesa sizes and thickness differences due to the number of stages employed. All of these improvements will contribute to reducing the K-factor.

V. Conclusion

5.1 Summary of Results

BC VCSELs with p-doped OAs have been successfully demonstrated for laser performance and high-frequency small-signal modulation performance. These are the first reported direct frequency response measurements of BC VCSELs [36].

At an operating temperature of -50 °C, the 3-stage BC VCSEL had a single-mode maximum output power $>$2 mW and a slope efficiency of 0.46 W/A. The 2-stage BC VCSEL had a single-mode maximum output power $>$2 mW and a slope efficiency of 0.36 W/A. Gigahertz performance of BC VCSELs at an operating temperature of -50 °C was demonstrated, with a maximum single-mode 3 dB frequency response $>$7 GHz and $>$5 GHz for a 3-stage and 2-stage BC VCSEL, respectively. Standard damping limitations, as well as thermal limitations, are clearly evident in the frequency response analysis. These limitations need to be overcome.

The quantifiable goals to demonstrate room-temperature high-speed BC VCSELs with (1) device slope efficiencies greater than 1 W/A, (2) small-signal modulation $>$5 GHz, and (3) improved impedance matching were not met. The 3-stage device operated at room temperature with a slope efficiency of 0.1 W/A and a -3 dB modulation bandwidth of 3.2 GHz. However, small-signal modulation exceeding 5 GHz was demonstrated at an operating temperature of -50 °C for both the 2- and 3-stage BC VCSELs. Significantly improved sloped efficiencies were also demonstrated, but did not meet the metric of 1 W/A. While not meeting the metric of 1 W/A the slope efficiencies are compare with the SOA for semiconductor lasers to date. Impedance matching became less of an issue after the BCL design was changed to a BC VCSEL. This is due to the small area of the device having a much larger resistance. This changed the effort from matching a low-resistance device to a high-resistance device. This will allow for the incorporation of a parallel matching circuit that is more robust and efficient than dumping the entire signal through a series matching load.

The demonstration at reduced temperatures of high-slope efficiency and high-frequency modulation BC VCSELs as well as limited operation at room-temperature of the 3-stage

BC VCSEL indicates that with further research a direct-drive RF photonic link is not only feasible, but can be a reality.

5.2 Future Work

Research opportunities exist for future work. While the 3-stage BC VCSELs do operate at room temperature, these BC VCSELs require design and material optimization to fulfill room-temperature high-speed ($>$ 10 GHz) performance with a slope efficiency $>$ 1 W/A. Investigations such as (1) optimizing the gain peak versus cavity tuning overlap to improve room temperature operation, (2) compositionally grading the DBR mirror layers to reduce interfacial band spikes, (3) investigating the optimum number of DBR mirror pairs used in a BC VCSEL to maximize the light output power as a function of number of stages used, and (4) specifically designed fabrication masks to minimize capacitance issues between mesa sizes and thickness differences due to the number of stages employed. The extension of high-speed operation to frequencies above 10 GHz at room temperature using BC VCSELs with very high slope efficiencies should be achievable.

Optimizing the cavity resonance and QW gain peak for room temperature operation and compositionally grading the DBR mirrors are important first steps to improve device performance. The cavity resonance - QW gain peak optimization would benefit by additional LIV characterization of the existing BC VCSELs at finer temperature levels to determine where the best alignment occurs. The QWs can then be adjusted by blue shifting the $In_{0.20}Ga_{0.80}As$ QW emission peak by reducing the QW thickness and/or reducing the indium concentration. Empirical values of 0.6 Å/°C and 0.1 Å/°C for the temperature shift of the QW gain peak and cavity resonance, respectively, have been used extensively [7, 46].

Along with tuning the gain peak to the cavity resonance, a detailed study to determine the optimal number of DBR mirrors for the desired stage is proposed. Since a 3-stage BC VCSEL has more round trip gain than a 2-stage BC VCSEL, the optimum number of DBR mirror pairs to maximize the power output will be less than the 2-stage BC VCSEL.

Modeling and simulating the effects of including a barrier (either a doped GaAs region of another OA layer) opposite the QW from the OA should give insight into why only one of the TJs band overlap with increased bias and not all of the TJs equally

Apart for BC VCSELs for RF photonic links, another opportunity for BC emitters is already underway. Taking advantage of the light uniformity and increased brightness by employing BC LEDs, resonant-cavity BC LEDs are currently being investigated as high-brightness narrow-waveband sources for an illuminator in a 3-D imaging system [43]. The broad area uniform illumination generated by incorporating tunnel junctions combined with the waveband narrowing and decreased divergence obtained using a resonant cavity design in an LED will significantly improve the signal-to-noise ratio of the illumination signal in even the brightest daytime ambient background situations.

5.3 Finale

Bipolar cascade lasers offer tremendous flexibility for numerous laser and high-brightness LED applications. Further improvement of BC VCSELs will provide significant advances in achieving and demonstrating a direct-drive RF photonic link system. Applying the bipolar cascade concept to LEDs will offer efficient and inexpensive illumination sources for numerous Air Force applications.

Appendix A. Gain-Guided Laser Process Follower

This is the in-house developed process follower for fabricating gain-guided edge-emitting lasers. It is single mask process designed to quickly fabricate a quarter of a two or three inch wafer. The follower includes four major sections: I. p-Contact Metallization, II. Wafer Thinning, III. Backside Metallization, and IV. Wafer Removal and Cleaning.

In Section I the wafer is photolithographically patterned with 2 cm long stripes with with stripe widths of 20 μm, 40 μm, 60 μm, 80 μm, and 100 μm. The top metal, consisting of Ti:Pt:Au (300 Å:500 Å:3500 Å) is evaporated and a liftoff is performed. The sample is RIE etched to remove the exposed p-cap to reduce lateral current spreading. The sample is then annealed at 410 °C for 15 s.

In Section II the sample is mounted upside down onto a lapping plate and the backside is thinned to a final thickness of $\sim$100 μm.

In Section III the backside metal is evaporated with a Ni:Ge:Au:Ni:Au (50 Å:170 Å: 330 Å:150 Å:3000 Å) metal layer profile and a liftoff is performed. The sample is then carefully removed from the lapping plate. The final step in this section is to anneal the thinned sample at 410 °C for 15 s.

In Section IV the processed sample is cleaved into 1 cm laser bars with cavity lengths of 200 μm, 250 μm, 330 μm, 400 μm, 500 μm, 660 μm and 800 μm.

Laser Process Follower

Quick Gain-Guided Lasers

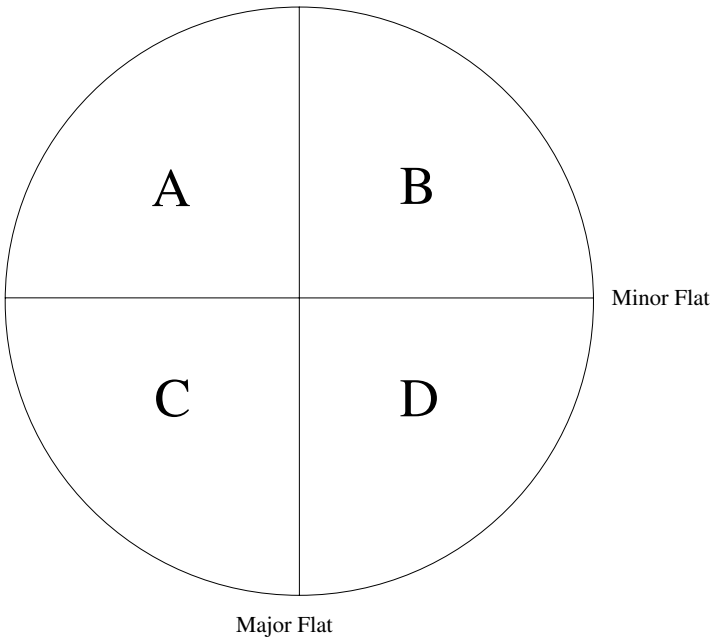
Ti-Pt-Au p^+ Contacts

Start Date: **8 August, 2007**

Piece ID:

Mesa Orient:

Notes on Piece:



I. *p*-Contact Metalization

8 August, 2007		Piece ID:	
Date Time	**Init.**	**Process**	**Notes**
		Prepare Wafer Surface ❑ Spin clean wafer with acetone, isopropyl alcohol, and DIW ❑ 30 seconds each @ 500 rpm ❑ N_2 blow dry ❑ 5 minute HPB @ 170° C *(evaporates accumulated H_2O)* ❑ Cool	
		PMGI Coat ❑ Set PMGI spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with PMGI SF-11 ❑ Spin 30 seconds @ 4000 rpm ❑ 5 minute HPB @ 270° C ❑ Cool	
		1813 Coat ❑ Set Photoresist Spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with 1813 ❑ Spin 30 seconds @ 4000 rpm ❑ 75 second HPB @ 110° C ❑ Cool	
		Wafer & Mask Inspection ❑ Inspect backside of wafer and gently clean with acetone and a swab ❑ Inspect **Laser Qualification Mask** ❑ Clean with acetone ❑ Rinse with isopropyl alcohol ❑ N_2 blow dry	
		Expose 1813 with LASER Qualification Mask ❑ Edge bead photoresist *(if desired)* Cover sample with Al foil mask MJB-3 expose, 365 nm, 45 sec (7 mW/cm^2) 50 second Spin Develop with 351:H_2O (1:5) @ 500 rpm 30 second DIW rinse N_2 blow dry Cover sample with Al foil mask 300 second DUV Exposure 240 nm (16.5 mW/cm^2) 30 second spin Develop with SAL 101 @ 500 rpm 30 second DIW rinse N_2 blow dry ❑ Align & expose **LASER Qualification Mask** MJB-3, 350 nm 20 seconds (7 mW/cm^2) *Ensure mask is aligned with the substrate crystal structure because the cleaving will follow the crystal structure and not the pattern processed onto the substrate!!!*	
		1813 Develop ❑ 30 second Spin Develop with 351:H_2O (1:5) @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Examine wafer alignment ❑ Examine to ensure 1813 developed	
		Expose PMGI ❑ 300 second DUV Exposure 240 nm (16.5 mW/cm^2).	
		PMGI Develop ❑ 30 second spin Develop with SAL 101 @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	

I. *p*-Contact Metalization

8 August, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
		Inspect Lithography ❑ Again, ensure wafer alignment is along crystal structure ❑ Examine to ensure PMGI developed	
		Descum ❑ 4 minute LFE Descum @ 200 W	
		Oxide removal directly prior to metalization ❑ 20 second DIP in BOE:DIW (1:10) ❑ DIW rinse in rinse tank (3 cycle minimum) ❑ N_2 blow dry	
		Metalization ❑ Evaporate 300 Å Ti 500 Å Pt 3500 Å Au	
		Tape-Liftoff ❑ Heat 1165 to ~100° C ❑ Lift off metal using wide tape ❑ Tape gold lift-off to bottom of page ❑ Use thin tape to clean-up remaining metal ❑ 30 second spray with acetone gun @ 500 rpm *Ensure all undesired metal is rinsed off* ❑ 30 second rinse with isopropyl alcohol @ 500 rpm ❑ Dry with N_2 @ 500 rpm ❑ Dry with N_2 on clean Texwipes ❑ Check backside & clean *(if necessary)*	
		PMGI Strip ❑ Strip PMGI in 100° C 1165 for approx. 4 minutes ❑ DIW rinse in rinse tank (6 cycles) ❑ N_2 blow dry.	
		Inspect Metalization ❑ Examine adhesion ❑ Examine metal edges *(look for wings, open areas, etc.)* ❑ Measure metal height on profilometer	Metal Step Hgt. _____ Å
		Descum ❑ 4 minute LFE Descum @ 200W	
		Rapid Thermal Anneal (RTA) ❑ 15 second RTA @ 410° C *(per RTA Standard Operating Procedures)*	
		Measure contact resistance of p^+ cap ❑ Measure stripe lengths if less than full mask *(if full mask the stripe length is 19 mm)* ❑ At probe station probe adjacent stripes 20 & 40, 40 & 60, 60 & 80, 80 & 100, 100 & 20 µm *(Note stripe numbers used for a, b, c,& d !!)* a_____ b_____ c_____ d_____ L_a_____mm L_b_____mm L_c_____mm L_d_____mm R_{1a}_____mΩ R_{2a}_____mΩ R_{3a}_____mΩ R_{4a}_____mΩ R_{5a}_____mΩ R_{1b}_____mΩ R_{2b}_____mΩ R_{3b}_____mΩ R_{4b}_____mΩ R_{5b}_____mΩ R_{1c}_____mΩ R_{2c}_____mΩ R_{3c}_____mΩ R_{4c}_____mΩ R_{5c}_____mΩ R_{1d}_____mΩ R_{2d}_____mΩ R_{3d}_____mΩ R_{4d}_____mΩ R_{5d}_____mΩ	
		Etch p^+ Cap ❑ 2.25 minute RIE Etch in ICP RIE *(no ICP power)* BCl_3:He (50 sccm:40 sccm), 20 mTorr, 100 W, DC bias 198 V ❑ Measure with profilometer to verify proper step height	Final Step Hgt. _____Å

II. Wafer Thinning

Date Printed: 8 August, 2007		Piece ID:	
Date Time	**Init.**	**Process** *(Check box when complete)*	**Notes**
		Bonding Wafer to Glass Flat ❑ Turn on and set Cleaning Station hot plate to 150° ❑ Put glass flat on hot plate and melt Crystal Bond wax ❑ Spread evenly leaving no gaps or large bubbles ❑ Wait about 1 minute for the bubbles to come out ❑ While flat remains on hot plate place substrate epi side down onto the center of the glass flat. *If placing more than 1 wafer or piece spread the pieces evenly over the glass flat.* ❑ Rotate and apply light pressure to evenly distribute wax ❑ Remove from heat and cool ❑ On spinner spray with acetone gun @ 500 rpm to remove excess wax	
The next 4 Steps will be done in the GaAs Wafer Processing Lab			
		Remove Excess Wax from Between Wafer and Glass Flat ❑ Turn on pump and hot plate *(for 150° C set hot plate to ~450)* ❑ Place glass flat on metal blank in vacuum chuck and set on hot plate ❑ Cover with filter paper ❑ Cover with vacuum compression chuck and let vacuum chuck heat to 150° C ❑ Draw vacuum *(As per vacuum chuck Standard Operating Procedures)* ❑ Remove vacuum chuck from hot plate and set on cooling plate keeping the vacuum chuck under vacuum ❑ Cool vacuum chuck to 40° C or less ❑ Open vacuum chuck *(As per vacuum chuck Standard Operating Procedures)* ❑ Remove vacuum chuck and filter paper ❑ Spray with acetone to remove excess wax ❑ Clean vacuum chuck of any remaining wax with acetone	
		Lapp substrate ❑ Measure initial wafer thickness above glass blank *Standard wafers are about 400 μm* ❑ Using 5 μm alumina grit, apply even pressure, lapp wafer until thickness is approximately 90 μm. ❑ Several stops and thickness measurements will be required ❑ Record final thickness	
		Polish Wafer ❑ Setup with felt polishing disk, 0.3 μm polishing grit and bleach ❑ Work grit and bleach into a wet paste ❑ Polish wafer until it has a mirror finish *Clorox always etches! Never wait more than 1 second to go from polishing pad to running water* ❑ Cleanup polishing hood ❑ Return 0.3 μm polishing grit and bleach	

III. Backside Metalization
(Back in the Cleanroom)

Date Printed: 8 August, 2007		**Piece ID:**	
Date Time	**Init.**	**Process** *(Check box when complete)*	**Notes**
		Clean Wafer & Glass Flat ❑ 30 second rinse with acetone @ 500 rpm ❑ Use Q-tip to gently remove any leftover grit from surface ❑ 30 second rinse with isopropyl alcohol @ 500 rpm ❑ 5 minute HPB @ 110° C ❑ Let blank cool.	
		Apply Positive Photoresist to Glass Flat ❑ With wafers still mounted onto the glass blank, paint photoresist on the glass blank and just over the edges of the substrate *Ensure the glass is completely covered and the wafer is not covered (except the edges of the wafer)* ❑ 10 minute HPB @ 110° C ❑ Cool ❑ Inspect for resist hardness and coverage	
		Descum ❑ 4 minute LFE Descum @ 200 W	
		Oxide removal directly prior to metalization ❑ 20 second DIP in BOE:DIW (1:10) ❑ DIW rinse in rinse tank (3 cycle minimum) ❑ N_2 blow dry	
		Metalization ❑ Evaporate *(standard S/D ohmic)* 50 Å Ni 170 Å Ge 330 Å Au 150 Å Ni 3000 Å Au	
		Tape-Liftoff ❑ Lift off metal using wide tape ❑ Tape gold lift-off to bottom of page ❑ Use thin tape to clean-up remaining metal ❑ 30 second spray with acetone gun @ 500 rpm *Ensure all undesired metal is rinsed off* ❑ 30 second rinse with isopropyl alcohol @ 500 rpm ❑ Dry with N_2 @ 500 rpm ❑ Dry with N_2 on clean Texwipe ❑ Check backside & clean *(if necessary*	

IV. Wafer Removal & Cleaving

Date Printed: 8 August, 2007		**Piece ID:**	
Date Time	**Init.**	**Process** *(Check box when complete)*	**Notes**
		Remove & Clean Wafer ❑ Set Cleaning Station hot plate to 150° C ❑ Heat glass blank to 150° C ❑ GENTLY slide wafer from holder onto heated aluminum foil ❑ GENTLY remove wafer from aluminum foil ❑ Turn off Cleaning Station hot plate ❑ Soak in acetone for 5 minutes *(Dissolves wax from front side of wafer)* ❑ 30 second spin rinse with acetone @ 500 rpm ❑ Soak in second acetone bath for 5 minutes ❑ 30 second spin rinse with isopropyl alcohol @ 500 rpm ❑ Soak in isopropyl alcohol for 1 minute ❑ GENTLY N_2 blow dry	
		Rapid Thermal Anneal (RTA) ❑ 15 second RTA @ 410° C *(per RTA Standard Operating Procedures)*	
		The final step will be done in the GaAs Wafer Processing Lab	
		Wafer Cleaving ❑ Cleave wafer 1 cm long by 800, 200, 660, 250, 500, 400, & 330 μm wide bars *(per Loomis LCD-1 Cleaving Machine Standard Operating Procedures)* ❑ Deliver to semiconductor laser testing lab ❑ Place in N_2 dry box for storage and inform tester	

Appendix B. High-Speed VCSEL Process Follower

This is the in-house developed process follower for fabricating high-speed ground-signal-ground *g-s-g* coplanar probable VCSELs. It is designed to fabricate a quarter of a three inch wafer. The follower includes seven major sections, some can be ignored if not necessary. These sections include: I. Backside Polishing *(not necessary if backside is already polished)*, II. Alignment Marks & Top Contact Metallization, III. Mesa Etch, IV. Bottom Contact Metallization, V. SU-8 textit(negative resist) Planarization & Aperture Opening, VI. Pad Metallization, and VII. Pad & Aperture Opening *(can be ignored if desired)*. Figure B.1 illustrates the complete layout of the mask design for a VCSEL with a 50 μm mesa.

Section I is an optional backside polishing. Sometimes material is grown on single-side polished wafers and polishing is very important for processing accuracy and to eliminate contamination. All in-house grown material is used double-side polished wafers and this step was not necessary for the BC VCSEL research.

Section II is a standard two-layer liftoff lithography defining alignment marks and the top contacts. This step uses a dark field mask and defines a half ring annulus designed to fit on mesas of various sizes ranging from 10 μm to 50 μm, Figure B.1a), the metal is evaporated.

Section III is a clear field mask defining the VCSEL mesas, Figure B.1b). This uses a silicon nitride layer as well as a two-layer resist lithography to fortify the mask during the dry etch. This etch takes advantage of a in-house developed reflectivity system allowing etch stop control on the order of 100 Å.

Section IV has several steps. The first step is a standard two-layer liftoff lithography to define the bottom contacts. This step uses a dark field mask and defines a half ring annulus around the base of the VCSEL mesa, opposite the top contact half-ring annulus, Figure B.1c). The bottom metal and backside metal is evaporated and the sample is annealed at 410 °C for 15 seconds in a forming gas (95% Ar - 5% H_2 environment. Initial characterization is then performed to qualify the material quality before progressing onto the oxidation. The oxidation is then accomplished in an in-house developed in-situ oxida-

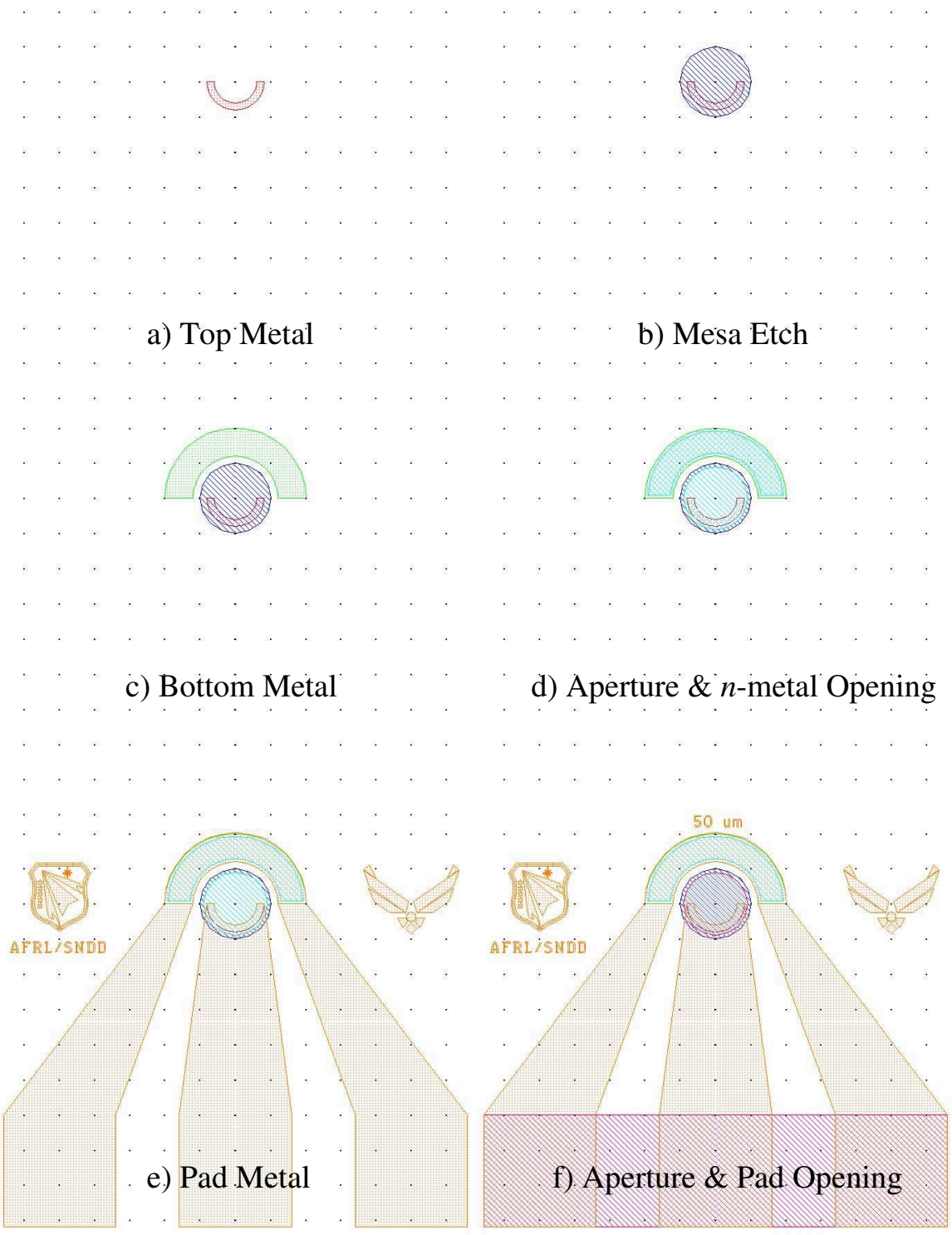


Figure B.1: High-speed VCSEL mask layout design for a VCSEL with a 50 μm mesa, a) is the top metal, b) is the mesa etch, c) is the bottom metal, d) is aperture and n-metal opening, e) is the pad metal, and f) is the aperture and pad opening.

tion furnace at 400 °C for up to five hours. Post-oxidation characterization is performed to determine VCSEL operational quality and to decide whether further oxidation is required.

Section V is an insulating and planarization step. Silicon nitride is applied to electrically insulate the side walls of the VCSEL mesa. It also ensures no further oxidation will occur eliminating some future reliability issues. The planarization step uses SU-8, which is a thick negative resit. A clear field mask defines the aperture on top of the VCSEL mesa, which also exposes the top contact, and the deep trench to expose the bottom contact, Figure B.1d). The exposed silicon nitride is dry etched to expose the top and bottom gold alloyed contacts.

Section VI is a standard two-layer liftoff lithography defining the metal *g-s-g* probe pads. This uses a dark field mask and defines the probe pads and the converging connections to the top and bottom ring annuli, Figure B.1e). The important requirement of this step is to sputter the metal to ensure step coverage down to the bottom contact. An extremely important lesson is to never use the tape liftoff technique after oxidation. The stress of the oxidized layer makes the mesas very susceptible to failure during a tape liftoff. Using the acetone liftoff ensures a high yield of working devices.

Section VII is a silicon nitride encapsulation feature. This is intended to reduce outgassing or water absorption of the SU-8. This water absorption can cause long-term failure due to temperature cycling. After the silicon nitride layer is deposited a standard two-layer lithography is performed and a dark field mask is used to define the aperture on top of the VCSEL mesa and the *g-s-g* probable pads, Figure B.1f).

Figure B.2 are micrographs of a 26 μm VCSEL. Figure B.2a) shows an optical micrograph, and Figure B.2b) is a scanning electron microscope (SEM) micrograph.

Figure B.2: Micrographs of a fully processed high-speed VCSEL. a) is an optical micrograph and b) is a scanning electron micrograph.

Laser Process Follower

Through DBR Contacted VCSEL

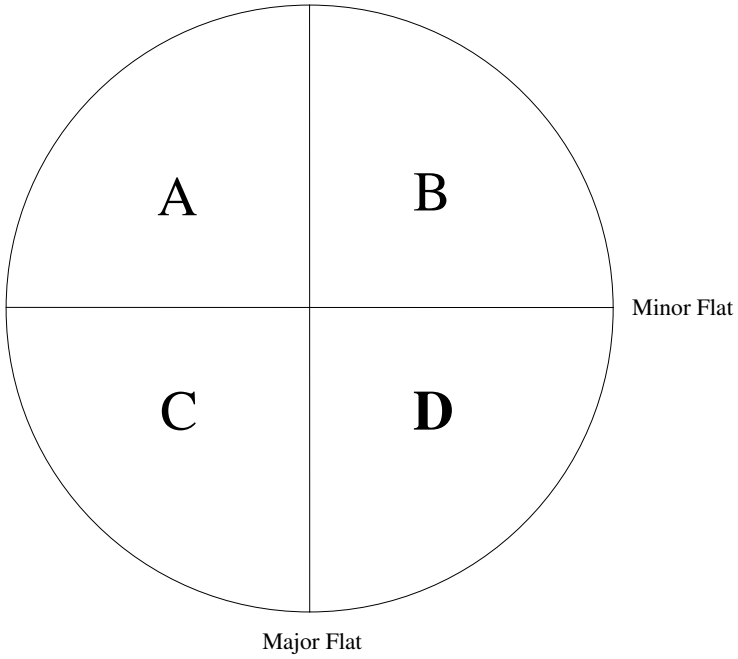
With Coplanar *g-s-g* High-Speed Probe Contact Pads

Start Date: **9 February, 2007**

Piece ID(s):

Mesa Orient:

Notes on Piece: TJ – *p*-doped OA – AR



Through DBR Contacted VCSEL with *g-s-g* Contact Pads			
9 February, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
I. Backside Polishing *(if necessary)*			
		Bonding Wafer to Glass Flat ❑ Turn on and set Cleaning Station hot plate to 150° ❑ Put glass flat on hot plate and melt Crystal Bond wax ❑ Spread evenly leaving no gaps or large bubbles ❑ Wait about 1 minute for the bubbles to come out ❑ While flat remains on hot plate place substrate epi side down onto the center of the glass flat. *If placing more than 1 wafer or piece spread the pieces evenly over the glass flat.* ❑ Rotate and apply light pressure to evenly distribute wax ❑ Remove from heat and cool ❑ On spinner spray with acetone gun @ 500 rpm to remove excess wax	
The next 2 Steps will be done in the GaAs Wafer Processing Lab			
		Remove Excess Wax from Between Wafer and Glass Flat ❑ Turn on pump and hot plate *(for 150°C set hot plate to ~450)* ❑ Place glass flat on metal blank in vacuum chuck and set on hot plate ❑ Cover with filter paper ❑ Cover with vacuum compression chuck and let vacuum chuck heat to 150° C ❑ Draw vacuum *(As per vacuum chuck Standard Operating Procedures)* ❑ Remove vacuum chuck from hot plate and set on cooling plate keeping the vacuum chuck under vacuum ❑ Cool vacuum chuck to 40° C or less ❑ Open vacuum chuck *(As per vacuum chuck Standard Operating Procedures)* ❑ Remove vacuum chuck and filter paper ❑ Spray with acetone to remove excess wax ❑ Clean vacuum chuck of any remaining wax with acetone	
		Polish Wafer ❑ Setup with felt polishing disk, 0.3 μm polishing grit and bleach ❑ Work grit and bleach into a wet paste ❑ Polish wafer until it has a mirror finish *Clorox always etches! Never wait more than 1 second to go from polishing pad to running water* ❑ Cleanup polishing hood ❑ Return 0.3 μm polishing grit and bleach	
		Remove & Clean Wafer (in Cleanroom) ❑ Set Cleaning Station hot plate to 150° C ❑ Heat glass blank to 150° C ❑ GENTLY slide wafer from holder onto heated aluminum foil ❑ GENTLY remove wafer from aluminum foil ❑ Soak in acetone for 5 minutes *(Dissolves wax from front side of wafer)* ❑ 30 second spin rinse with acetone @ 500 rpm ❑ Soak in second acetone bath for 5 minutes ❑ 30 second spin rinse with isopropyl alcohol @ 500 rpm ❑ Soak in isopropyl alcohol for 1 minute ❑ 30 second spin rinse with isopropyl alcohol @ 500 rpm ❑ GENTLY N_2 blow dry. ❑ Turn off Cleaning Station hot plate	

Through DBR Contacted VCSEL with *g-s-g* Contact Pads			
9 February, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
II. Alignment & Top Contact Metal			
		Prepare Wafer Surface ❑ Spin clean wafer with ACE, IPA, and DIW 30 seconds each @ 500 rpm ❑ N_2 blow dry ❑ 2 minute hot plate bake (HPB) @ 110° C *(removes accumulated H_2O)* ❑ Cool	
		PMGI Coat ❑ Set PMGI spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with PMGI SF-11 ❑ Spin 30 seconds @ 4000 rpm ❑ 5 minute HPB @ 270° C ❑ Cool	
		1813 Coat ❑ Set photoresist spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with 1813 ❑ Spin 30 seconds ❑ 75 second HPB @ 110° C ❑ Cool	
		Wafer & Mask Inspection ❑ Inspect backside of wafer and gently clean with acetone and a swab ❑ Inspect **AFRL HS VCSEL MASK #1 Align. Marks & Top Metal** ❑ Clean with ACE ❑ Rinse with IPA ❑ N_2 blow dry	
		Expose 1813 with AFRL HS VCSEL MASK #1 Align. Marks & Top Metal ❑ Edge bead photoresist *(if desired)* Cover sample with Al foil mask MJB-3 expose, 365 nm, 30 sec (7 mW/cm^2) 30 second Spin Develop with 351:H_2O (1:5) @ 500 rpm 30 second DIW rinse N_2 blow dry For PMGI – Cover sample with Al foil mask 300 second DUV Exposure 240 nm (16.5 mW/cm^2) 30 second spin Develop with SAL 101 @ 500 rpm 30 second DIW rinse N_2 blow dry ❑ Align & expose **AFRL HS VCSEL MASK #1 Align. Marks & Top Metal** MJB-3, 405 nm, 20 seconds (7 mW/cm^2) *Ensure mask is aligned with the substrate crystal structure because any cleaving will follow the crystal structure and not the pattern processed onto the substrate!!!*	
		1813 Develop ❑ 30 second Spin Develop with 351: H_2O (1:5) @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Examine wafer alignment ❑ Examine to ensure 1813 developed	
		Expose PMGI ❑ 300 second DUV Exposure 240 nm (16.5 mW/cm^2).	
		PMGI Develop ❑ 30 second spin Develop with SAL 101 @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Again, ensure wafer alignment is along crystal structure	

Through DBR Contacted VCSEL with *g-s-g* Contact Pads			
9 February, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
		❑ Examine to ensure PMGI developed	
		Descum ❑ 4 minute LFE Descum @ 200W	
		Oxide Removal Prior to Metal Deposition ❑ 20 second DIW:BOE (10:1) dip ❑ DIW rinse in rinse tank (3 cycles) ❑ N_2 blow dry	
		Metalization ❑ Evaporate patterned side of the sample For a *p-i-n* structure 300 Å Ti 500 Å Pt 3500 Å Au or for a cascade laser 50 Å Ni 170 Å Ge 330 Å Au 150 Å Ni 3000 Å Au	
		Tape-Liftoff ❑ Heat 1165 to ~100° C ❑ Lift off metal using wide tape ❑ Tape gold lift-off to bottom of page ❑ Lift off with Scotch tape (in one direction) ❑ Rotate sample 90° ❑ Lift off with Scotch tape (in one direction) ❑ 15 second spray with acetone gun @ 500 rpm *Ensure all undesired metal is rinsed off* ❑ 15 second rinse with IPA @ 500 rpm ❑ Strip PMGI in 100° C 1165 for approx. 4 minutes ❑ DIW rinse in rinse tank (6 cycles) ❑ N_2 blow dry	
		Inspect Metalization ❑ Examine adhesion ❑ Examine metal edges *(look for wings, open areas, etc.)* ❑ Measure metal height on profilometer	Metal Step Hgt. _____ Å
		Descum ❑ 4 minute LFE Descum @ 200W	
III. Top Mesa			
		Prepare Wafer Surface ❑ Spin clean wafer with ACE and IPA 30 seconds each @ 500 rpm ❑ N_2 blow dry ❑ 2 minute hot plate bake (HPB) @ 110° C *(removes accumulated H_2O)* ❑ Cool	
		Si_3N_4 Deposition ❑ Sputter or PECVD 5000 Å Si_3N_4	
		PMGI Coat ❑ Set PMGI spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with PMGI SF-11 ❑ Spin 30 seconds @ 4000 rpm ❑ 5 minute HPB @ 270° C ❑ Cool	
		1813 Coat ❑ Set photoresist spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with 1813 ❑ Spin 30 seconds ❑ 75 second HPB @ 110° C ❑ Cool	
		Wafer & Mask Inspection ❑ Inspect backside of wafer and gently clean with acetone and a swab ❑ Inspect **AFRL HS VCSEL MASK #2, Mesa**	

Through DBR Contacted VCSEL with *g-s-g* Contact Pads			
9 February, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
		❑ Clean with ACE ❑ Rinse with IPA ❑ N_2 blow dry	
		Expose 1813 with AFRL HS VCSEL MASK #2, Mesa ❑ Edge bead photoresist *(if desired)* Cover sample with Al foil mask MJB-3 expose, 365 nm, 30 sec (7 mW/cm^2) 30 second Spin Develop with 351:H_2O (1:5) @ 500 rpm 30 second DIW rinse N_2 blow dry For PMGI – Cover sample with Al foil mask 300 second DUV Exposure 240 nm (16.5 mW/cm^2) 30 second spin Develop with SAL 101 @ 500 rpm 30 second DIW rinse N_2 blow dry ❑ Align & expose **AFRL HS VCSEL MASK #2, Mesa** MJB-3, 405 nm, 20 seconds (7 mW/cm^2) *Ensure mask is aligned with the substrate crystal structure because any cleaving will follow the crystal structure and not the pattern processed onto the substrate!!!*	
		1813 Develop ❑ 30-60 second puddle & spin develop with 351: H_2O (1:5) @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Examine to ensure 1813 developed	
		Expose PMGI ❑ 300 second DUV Exposure 240 nm (16.5 mW/cm^2).	
		PMGI Develop ❑ 30-60 second puddle & spin Develop with SAL 101 @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Examine to ensure PMGI developed	
		Descum ❑ 4 minute LFE Descum @ 200W	
		Step Height Profile Prior to Mesa RIE etch ❑ Measure step height using TENCOR profilometer	Resist Step Height _____ μm
		Si_3N_4 RIE Etch ❑ Anisotropically etch Si_3N_4 in Dual Chamber RIE 30 minutes with Freon 23:O_2 (45 sccm:3 sccm) and Ardel Platen	
		Step Height Profile After Si_3N_4 RIE etch ❑ Measure step height using TENCOR profilometer	Etch & Resist Height _____ μm
		Mesa RIE Etch ❑ Set up reflectance monitoring equipment on ICP etcher ❑ PC - double click on RIE Reflectance ❑ Change time interval to 0.01 seconds ❑ Mount sample on sapphire holder using diffusion pump oil (*use a SMALL amount of oil, but not too small, otherwise it will contaminate wafer surface!)* ❑ Anisotropically etch in ICP System to desired depth using reflectance signal BCl_3:Cl (30 sccm: 10 sccm), 600W ICP, 60 W RIE, Temps 17° C & 10° C, 4 mTorr, 9 sccm He ❑ Clean wafer and sapphire holder using IPA	
		Post ICP RIE Step Height Measurement ❑ Measure step height using TENCOR profilometer	Step Height _____ μm

Through DBR Contacted VCSEL with *g-s-g* Contact Pads			
9 February, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
		PMGI Strip ❑ Heat 1165 to ~100° C ❑ 30 second spray with ACE @ 500 rpm ❑ 30 second rinse with IPA @ 500 rpm ❑ Strip PMGI in 100° C 1165 for 4-5 minutes ❑ DIW rinse in rinse tank (4-6 cycles) ❑ N_2 blow dry	
		Descum ❑ 4 minute LFE Descum @ 200W	
		Step Height Profile After PMGI Removal ❑ Measure step height using TENCOR profilometer	Step Height _____ μm
		Inspect Etch ❑ Examine to ensure sample etched properly and mesa definition is good	
		Si_3N_4 RIE Etch ❑ Isotropically etch Si_3N_4 in Dual Chamber RIE 10' with Freon 14:O_2 (45 sccm: 2 sccm) and Aluminum Platen	
		Post Si_3N_4 RIE Step Height Measurement ❑ Measure step height using TENCOR profilometer	Step Height _____ μm
IV. Bottom Contact Metallization			
		Prepare Wafer Surface ❑ Spin clean wafer with ACE, IPA, & DIW 30 seconds each @ 500 rpm ❑ N_2 blow dry ❑ 2 minute hot plate bake (HPB) @ 110° C *(removes accumulated H_2O)* ❑ Cool	
		PMGI Coat ❑ Set PMGI spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with PMGI SF-11 ❑ Spin 30 seconds @ 4000 rpm ❑ 5 minute HPB @ 270° C ❑ Cool	
		1813 Coat ❑ Set photoresist spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with 1818 ❑ Spin 30 seconds ❑ Inspect backside of wafer and gently clean with acetone and a swab ❑ 75 second HPB @ 110° C ❑ Cool	
		Wafer & Mask Inspection ❑ Inspect backside of wafer and gently clean with acetone and a swab ❑ Inspect **AFRL HS VCSEL MASK #3 Bottom Metal** ❑ Clean with acetone ❑ Rinse with isopropyl alcohol ❑ N_2 blow dry	
		Expose 1813 with AFRL HS VCSEL MASK #3 Bottom Metal ❑ Edge bead photoresist *(if desired)* Cover sample with Al foil mask MJB-3 expose, 365 nm, 30 sec (7 mW/cm^2) 30 second Spin Develop with 351:H_2O (1:5) @ 500 rpm 30 second DIW rinse N_2 blow dry For PMGI – Cover sample with Al foil mask 300 second DUV Exposure 240 nm (16.5 mW/cm^2) 30 second spin Develop with SAL 101 @ 500 rpm 30 second DIW rinse	

Through DBR Contacted VCSEL with *g-s-g* Contact Pads			
9 February, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
		N_2 blow dry ❑ Align & expose **AFRL HS VCSEL MASK #3 Bottom Metal** MJB-3, 405 nm, 20 seconds (7 mW/cm^2)	
		1813 Develop ❑ 30 second Spin Develop with 351: H_2O (1:5) @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Examine wafer alignment ❑ Examine to ensure 1818 developed	
		Expose PMGI ❑ 300 second DUV Exposure 240 nm (16.5 mW/cm^2).	
		PMGI Develop ❑ 45 second puddle/spin Develop with SAL 101 @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Again, ensure wafer alignment is along crystal structure ❑ Examine to ensure PMGI developed	
		Descum ❑ 4 minute LFE Descum @ 200W	
		Oxide Removal Prior to Metal Deposition ❑ 20 second DIW:BOE (10:1) dip ❑ DIW rinse in rinse tank (3 cycles) ❑ N_2 blow dry	
		***n*-ohmic Metalization** ❑ Evaporate the patterned side 50 Å Ni 170 Å Ge 330 Å Au 150 Å Ni 3000 Å Au ❑ Flip samples and evaporate the backside 50 Å Ni 170 Å Ge 330 Å Au 150 Å Ni 3000 Å Au	
		Tape-Liftoff ❑ Heat 1165 to ~100° C ❑ Lift off metal using wide tape ❑ Tape gold lift-off to bottom of page ❑ Lift off with Scotch tape (in one direction) ❑ Rotate sample 90° ❑ Lift off with Scotch tape (in one direction) ❑ 15 second spray with acetone gun @ 500 rpm *Ensure all undesired metal is rinsed off* ❑ 15 second rinse with isopropyl alcohol @ 500 rpm ❑ Strip PMGI in 100° C 1165 for approx. 4 minutes ❑ DIW rinse in rinse tank (6 cycles) ❑ N_2 blow dry	
		Inspect Metalization ❑ Examine adhesion ❑ Examine metal edges *(look for wings, open areas, etc.)* ❑ Measure metal height on profilometer	Metal Step Hgt. _____ Å
		Descum ❑ 4 minute LFE Descum @ 200W	
		Rapid Thermal Anneal ❑ 15 second RTA @ 410° C *(per RTA Standard Operating Procedures)*	
The next step will be performed in the OE Testing Laboratory			
		Preliminary VCSEL testing & Oxidation in OE Lab ❑ Perform preliminary VCSEL testing at VCSEL Testing Station ❑ Oxidize samples @ 400° C using the *In-situ* oxidation furnace per SOPs	

Through DBR Contacted VCSEL with *g-s-g* Contact Pads			
9 February, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
		❑ Perform follow-on VCSEL testing at VCSEL Testing Station	
V. SU-8 (negative resist) Planarization & Aperture Opening			
		Prepare Wafer Surface ❑ Spin clean wafer with ACE & IPA 30 seconds each @ 500 rpm ❑ N_2 blow dry ❑ 2 minute hot plate bake (HPB) @ 110° C *(removes accumulated H_2O)* ❑ Cool	
		Si_3N_4 Deposition ❑ Sputter or PECVD 5000 Å Si_3N_4	
		SU-8 Coat (Negative Resist) ❑ Set photoresist spinner ramp = 999 5.0 µm SU-8 2005 **spread = 500 rpm for 5 sec, spin = 3000 rpm for 30 sec** 7.5 µm SU-8 2005 **spread = 500 rpm for 5 sec, spin = 1000 rpm for 30 sec** 10.0 µm SU-8 2010 **spread = 500 rpm for 8 sec, spin = 3000 rpm for 30 sec** 12.5 µm SU-8 2010 **spread = 500 rpm for 8 sec, spin = 2000 rpm for 30 sec** ❑ Flood wafer with desired SU-8 ❑ Spin SU-8 for desired thickness ❑ Wipe backside of wafer with acetone soaked wipe while on spinner ❑ 1' air bake on spinner ❑ Clean backside with EBR dampened swab *(if necessary)* ❑ 3' HPB @ 65° C ❑ 3' HPB @ 110° C ❑ Cool sample	
		Wafer & Mask Inspection ❑ Inspect backside of wafer and gently clean with acetone and a swab ❑ Inspect **AFRL HS VCSEL MASK #4 Aperture** ❑ Clean with acetone ❑ Rinse with isopropyl alcohol ❑ N_2 blow dry	
		Expose SU-8 with AFRL HS VCSEL MASK #4 Aperture ❑ Align & expose **AFRL HS VCSEL MASK #4 Aperture** MJB-3, 365 nm, 10 seconds (7 mW/cm^2)	
		Post Exposure Bake ❑ 3' HPB @ 65° C ❑ 3' HPB @ 110° C ❑ Cool sample	
		SU-8 Develop ❑ Bucket Develop with SU-8 developer for at least 3' ❑ 15 second IPA rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Examine wafer alignment ❑ Ensure SU-8 developed, make sure features are open, clean, and sharp	
		Post Develop Bake ❑ 2' HPB @ 270° C	
		Descum ❑ 4 minute LFE Descum @ 200W	
		Step Height Profile Prior to Mesa RIE etch ❑ Measure step height using TENCOR profilometer	Resist Step Height _____ µm

Through DBR Contacted VCSEL with *g-s-g* Contact Pads			
9 February, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
		Si_3N_4 RIE Etch ❑ Anisotropically etch Si_3N_4 in Dual Chamber RIE 30 minutes with Freon 23:O_2 (45 sccm:3 sccm) and Ardel Platen	
		Step Height Profile After Si_3N_4 RIE etch ❑ Measure step height using TENCOR profilometer	Etch & Resist Height _____ μm
VI. Pad Metalization			
		Prepare Wafer Surface ❑ Spin clean wafer with acetone, isopropyl alcohol, and DIW 30 seconds each @ 500 rpm ❑ N_2 blow dry ❑ 2 minute hot plate bake (HPB) @ 110° C *(removes accumulated H_2O)* ❑ Cool	
		PMGI Coat ❑ Set PMGI spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with PMGI SF-11 ❑ Spin 30 seconds @ 4000 rpm ❑ 5 minute HPB @ 270° C ❑ Cool	
		1813 Coat ❑ Set photoresist spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with 1813 ❑ Spin 30 seconds ❑ Inspect backside of wafer and gently clean with acetone and a swab ❑ 75 second HPB @ 110° C ❑ Cool	
		Wafer & Mask Inspection ❑ Inspect backside of wafer and gently clean with acetone and a swab ❑ Inspect **AFRL HS VCSEL MASK #5 Pad Metal** ❑ Clean with acetone ❑ Rinse with isopropyl alcohol ❑ N_2 blow dry	
		Expose 1813 with AFRL HS VCSEL MASK #5 Pad Metal ❑ Edge bead photoresist *(if desired)* Cover sample with Al foil mask MJB-3 expose, 365 nm, 30 sec (7 mW/cm^2) 30 second Spin Develop with 351:H_2O (1:5) @ 500 rpm 30 second DIW rinse N_2 blow dry ❑ Align & expose **AFRL HS VCSEL MASK #5 Pad Metal** MJB-3, 405 nm, 15 seconds (7 mW/cm^2)	
		1813 Develop ❑ 30 second Spin Develop with 351: H_2O (1:5) @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Examine to ensure 1813 developed	
		Expose PMGI ❑ 300 second DUV Exposure 240 nm (16.5 mW/cm^2).	
		PMGI Develop ❑ 30 second spin Develop with SAL 101 @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Examine to ensure PMGI developed	
		Descum	

Through DBR Contacted VCSEL with *g-s-g* Contact Pads			
9 February, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
		❑ 4 minute LFE Descum @ 200W	
		Metalization ❑ Sputter 200 Å Ti 4000 Å Au	
		Acetone Liftoff ❑ Heat 1165 to ~100° C ❑ Spray with acetone gun @ 500 rpm *Ensure all undesired metal is rinsed off* ❑ 15 second rinse with isopropyl alcohol @ 500 rpm ❑ Strip PMGI in 100° C 1165 for approx. 4 minutes ❑ DIW rinse in rinse tank (6 cycles) ❑ N_2 blow dry	
		Inspect Metalization ❑ Examine adhesion ❑ Examine metal edges *(look for wings, open areas, etc.)* ❑ Measure metal height on profilometer	Metal Step Hgt. _____ Å
		Descum ❑ 4 minute LFE Descum @ 200W	
VII. Pad & Aperture Opening			
		Prepare Wafer Surface ❑ Spin clean wafer with acetone, isopropyl alcohol, and DIW 30 seconds each @ 500 rpm ❑ N_2 blow dry ❑ 2 minute hot plate bake (HPB) @ 110° C *(removes accumulated H_2O)* ❑ Cool	
		Si_3N_4 Deposition ❑ Sputter or PECVD 5000 Å Si_3N_4	
		1813 Coat ❑ Set photoresist spinner ramp rate = 200; spin = 4000 rpm ❑ Flood wafer with 1813 ❑ Spin 30 seconds ❑ Inspect backside of wafer and gently clean with acetone and a swab ❑ 75 second HPB @ 110° C ❑ Cool	
		Wafer & Mask Inspection ❑ Inspect backside of wafer and gently clean with acetone and a swab ❑ Inspect **AFRL HS VCSEL MASK #6 Open** ❑ Clean with acetone ❑ Rinse with isopropyl alcohol ❑ N_2 blow dry	
		Expose 1813 with AFRL HS VCSEL MASK #6 Open ❑ Edge bead photoresist *(if desired)* Cover sample with Al foil mask MJB-3 expose, 365 nm, 30 sec (7 mW/cm^2) 30 second Spin Develop with 351:H_2O (1:5) @ 500 rpm 30 second DIW rinse N_2 blow dry ❑ Align & expose **AFRL HS VCSEL MASK #6 Open** MJB-3, 405 nm, 15 seconds (7 mW/cm^2)	
		1813 Develop ❑ 30 second spin develop with 351:H_2O (1:5) @ 500 rpm ❑ 30 second DIW rinse ❑ N_2 blow dry	
		Inspect Lithography ❑ Examine to ensure 1813 developed	
		Descum	

Through DBR Contacted VCSEL with *g-s-g* Contact Pads			
9 February, 2007		**Piece ID:**	
Date Time	**Init.**	**Process**	**Notes**
		❑ 4 minute LFE Descum @ 200W	
		Step Height Profile Prior to RIE etch ❑ Measure step height using TENCOR profilometer	Step Height _____ μm
		Si_3N_4 RIE Etch ❑ Isotropically etch Si_3N_4 in Dual Chamber RIE 10 minutes with Freon 14:O_2 (45 sccm:2 sccm) and Al Platen	
		1813 Strip ❑ Spray with Acetone Gun@ 500 rpm (as necessary) ❑ Spin clean wafer with acetone, isopropyl alcohol, and DIW 30 seconds each @ 500 rpm ❑ N_2 blow dry	
		Descum ❑ 4 minutes LFE Descum @ 200W to ensure photoresist is completely removed	
		Step Height Profile After Resist Removal ❑ Measure step height using TENCOR profilometer	Step Height _____ μm

Appendix C. Multiple Stage Quad Charts

This appendix details device characterization by comparing 1-, 2-, and 3-stage BC VCSELs. The characterization is provided in a quad chart format for every mesa size and temperature. Chart a) illustrates the light power versus drive current (LI), chart b) the light power versus drive power (LD), chart c) the voltage versus drive current (VI), and chart d) the frequency response. The color scheme is identical for all quad charts. The 3-stage devices are blue, the 2-stage devices are red, and the 1-stage devices are black. The vertical lines in the LI chart, chart a), indicates the operating current for the best performing frequency response shown in the frequency response chart in d).

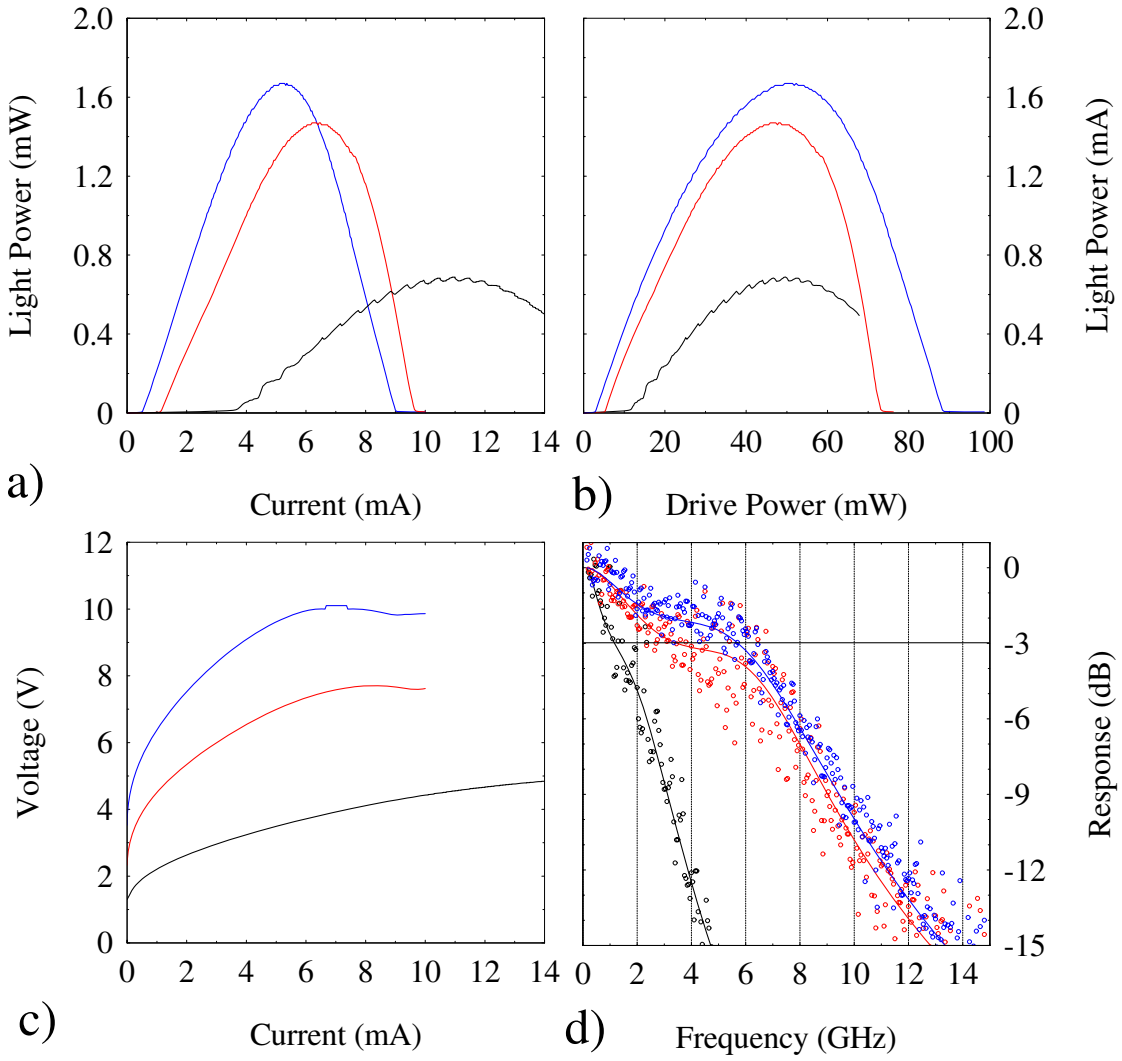


Figure C.1: Operating characteristics for 24 μm mesa 1- (black), 2- (red), and 3-stage (blue) BC VCSELs at a mount temperature of -50 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

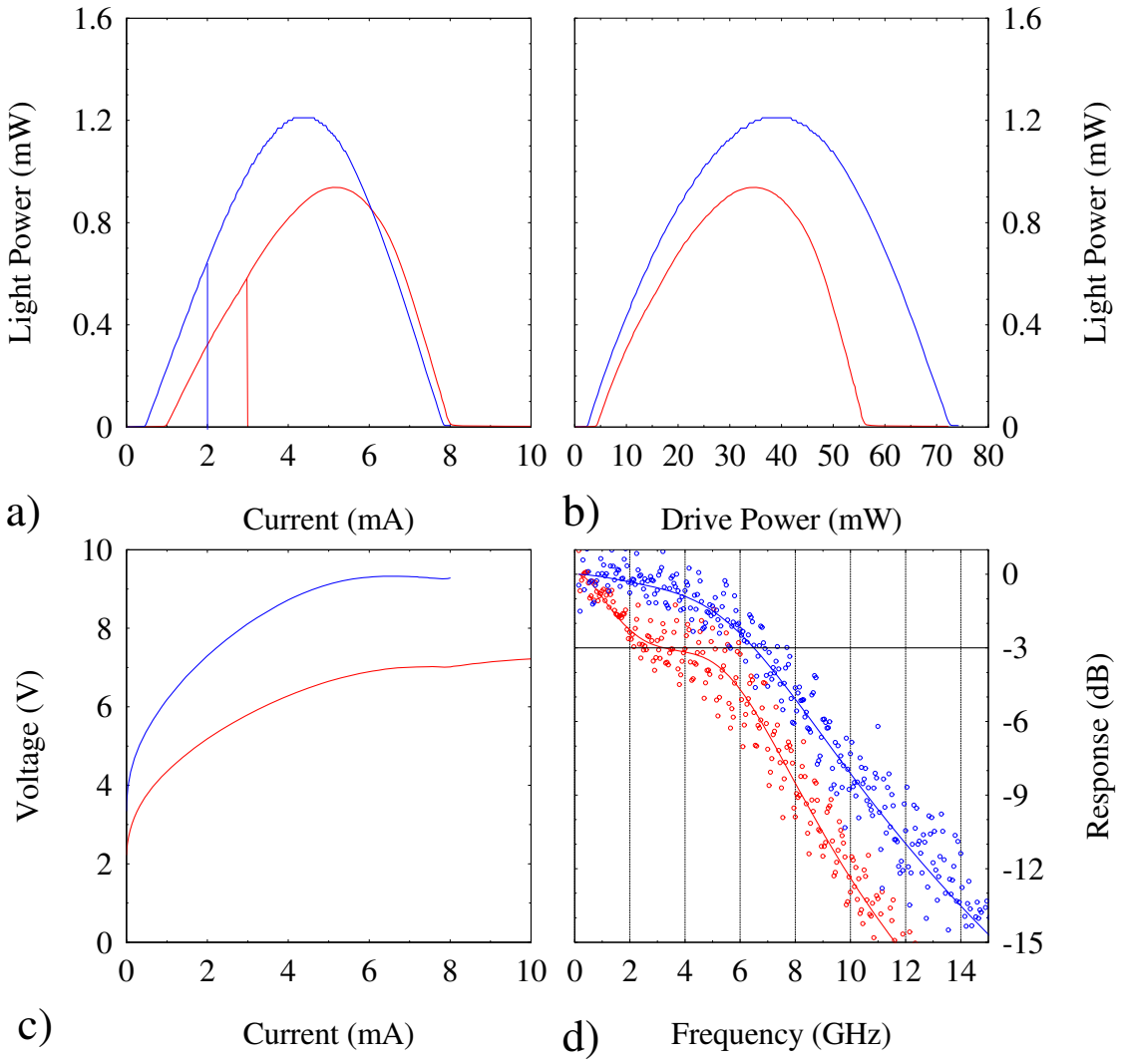


Figure C.2: Operating characteristics for 24 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of -25 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

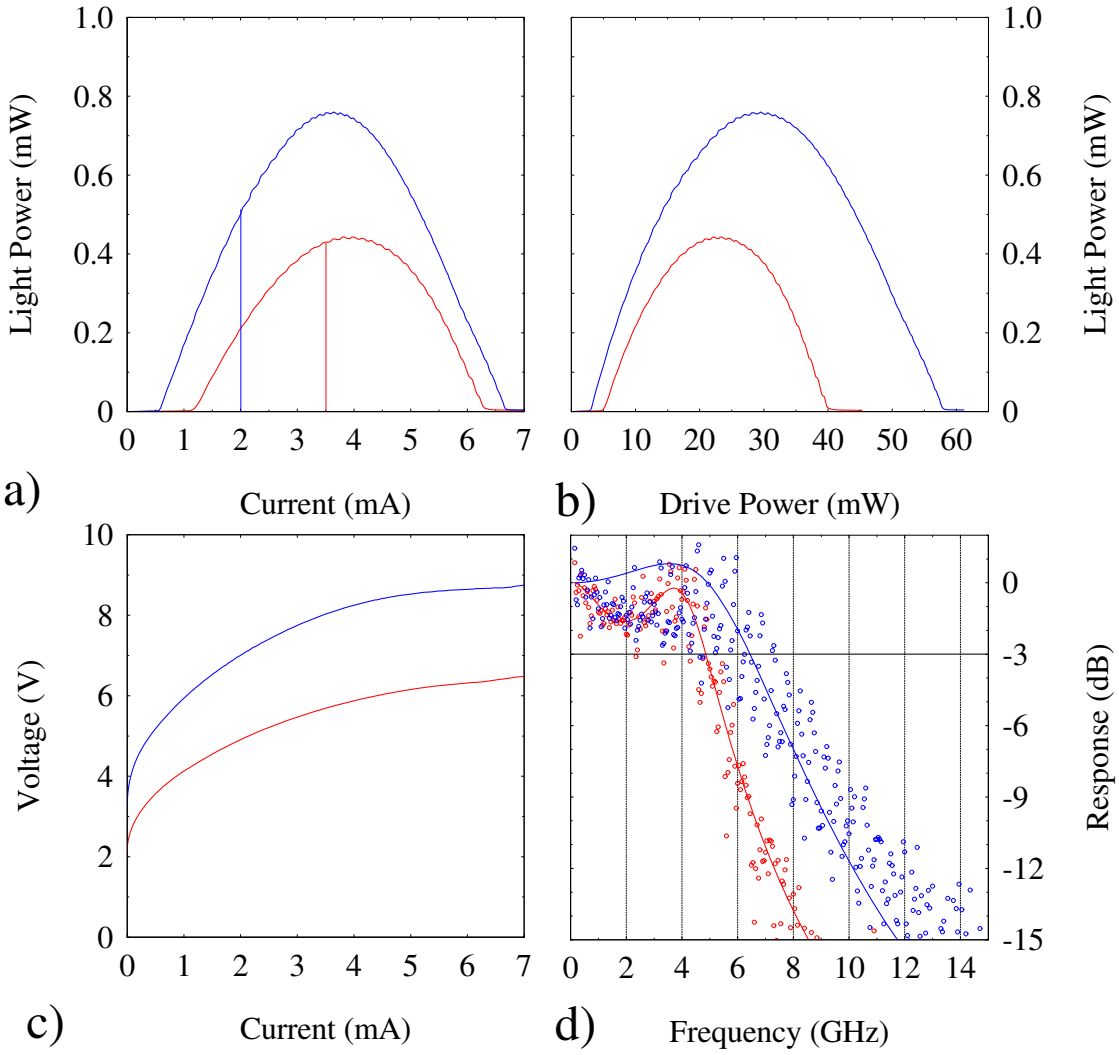


Figure C.3: Operating characteristics for 24 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of 0 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

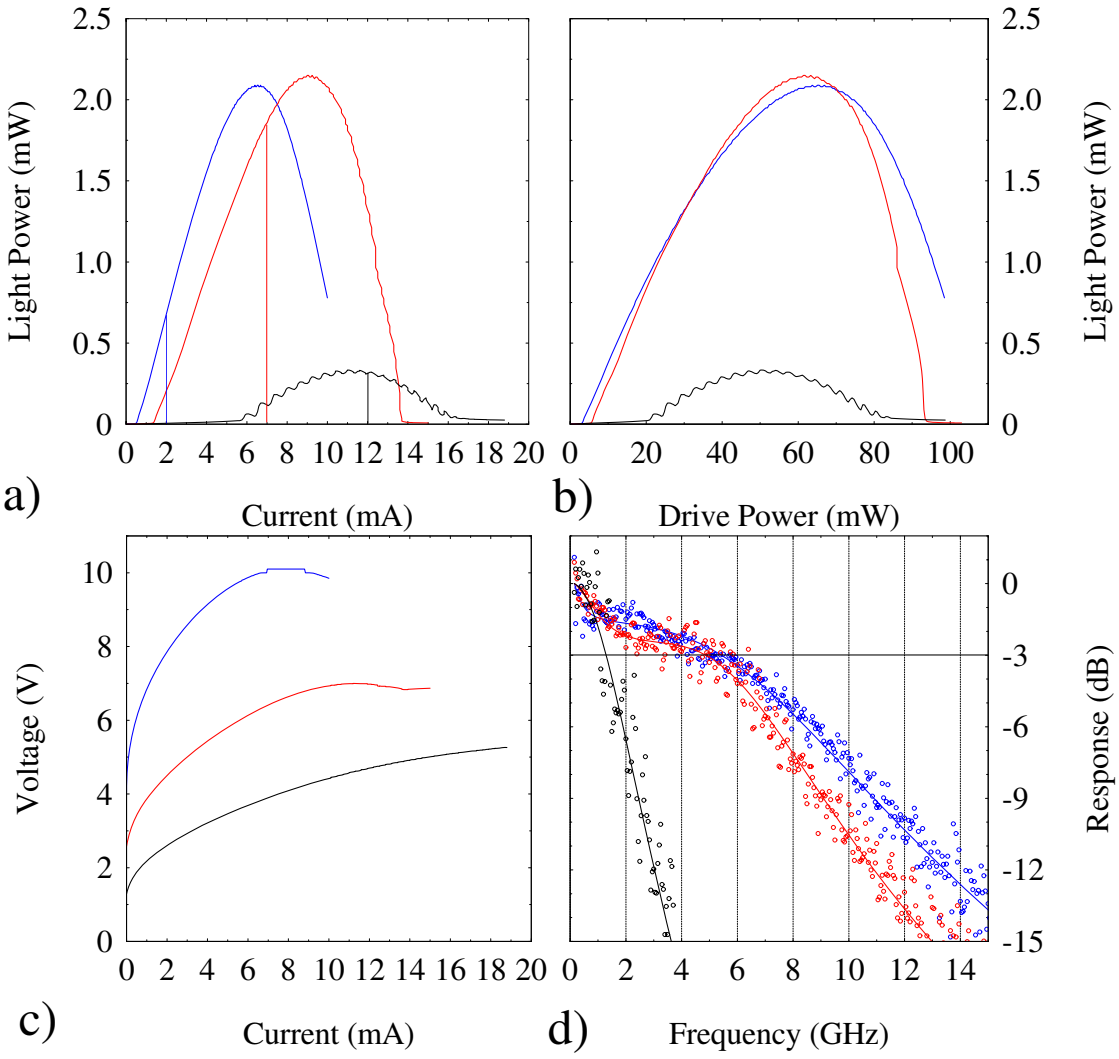


Figure C.4: Operating characteristics for 26 μm mesa 1- (black), 2- (red), and 3-stage (blue) BC VCSELs at a mount temperature of -50 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

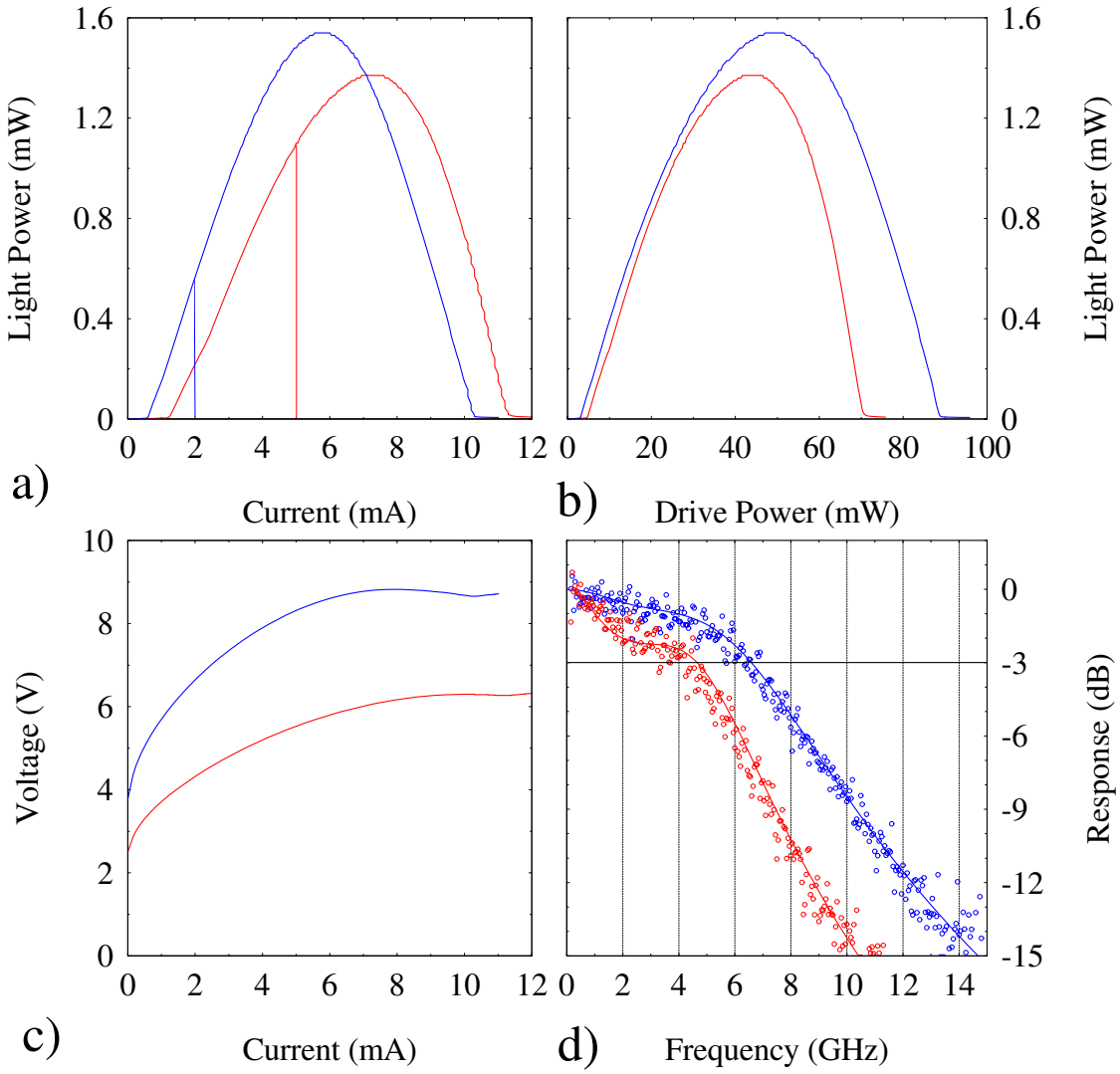


Figure C.5: Operating characteristics for 26 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of -25 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

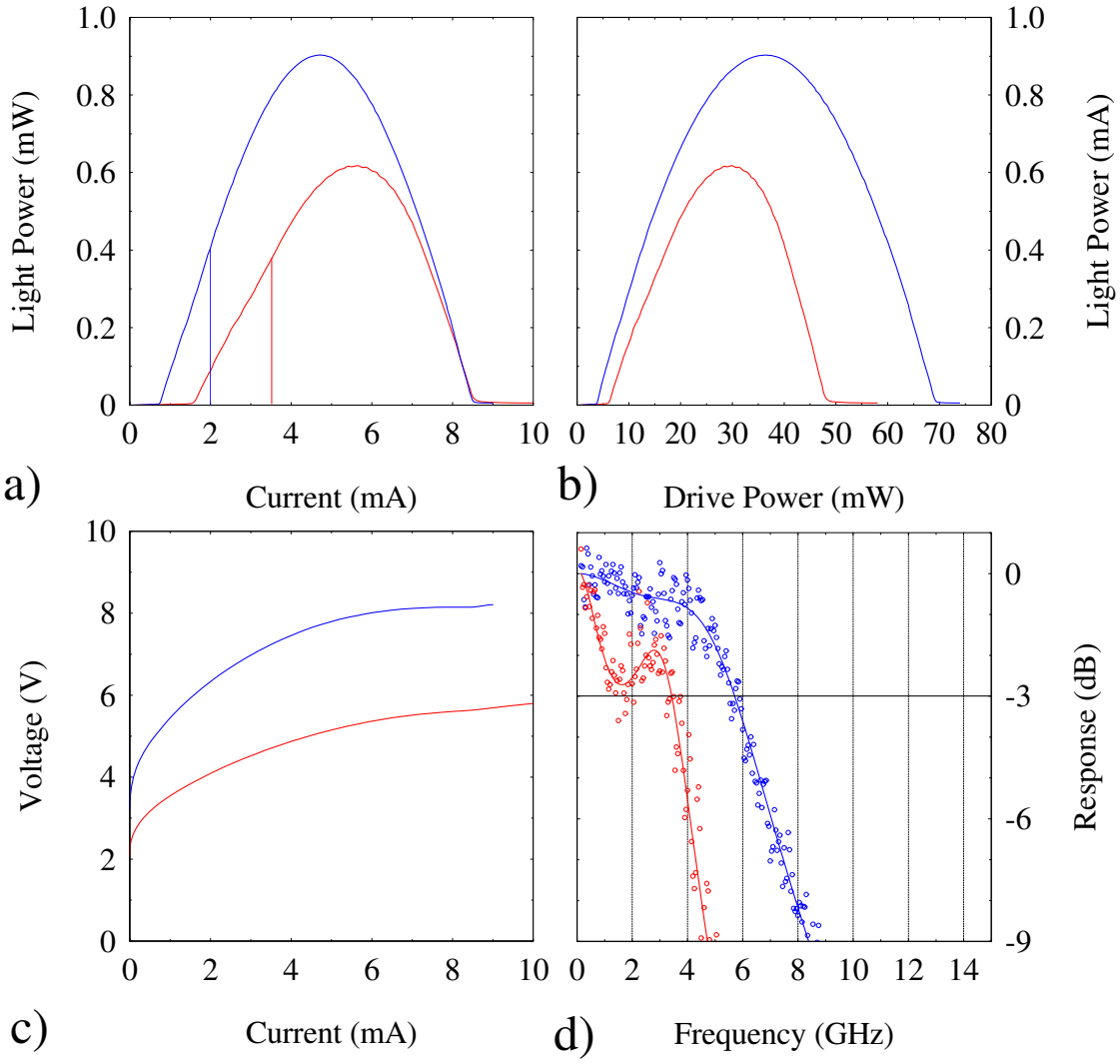


Figure C.6: Operating characteristics for 26 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of 0 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

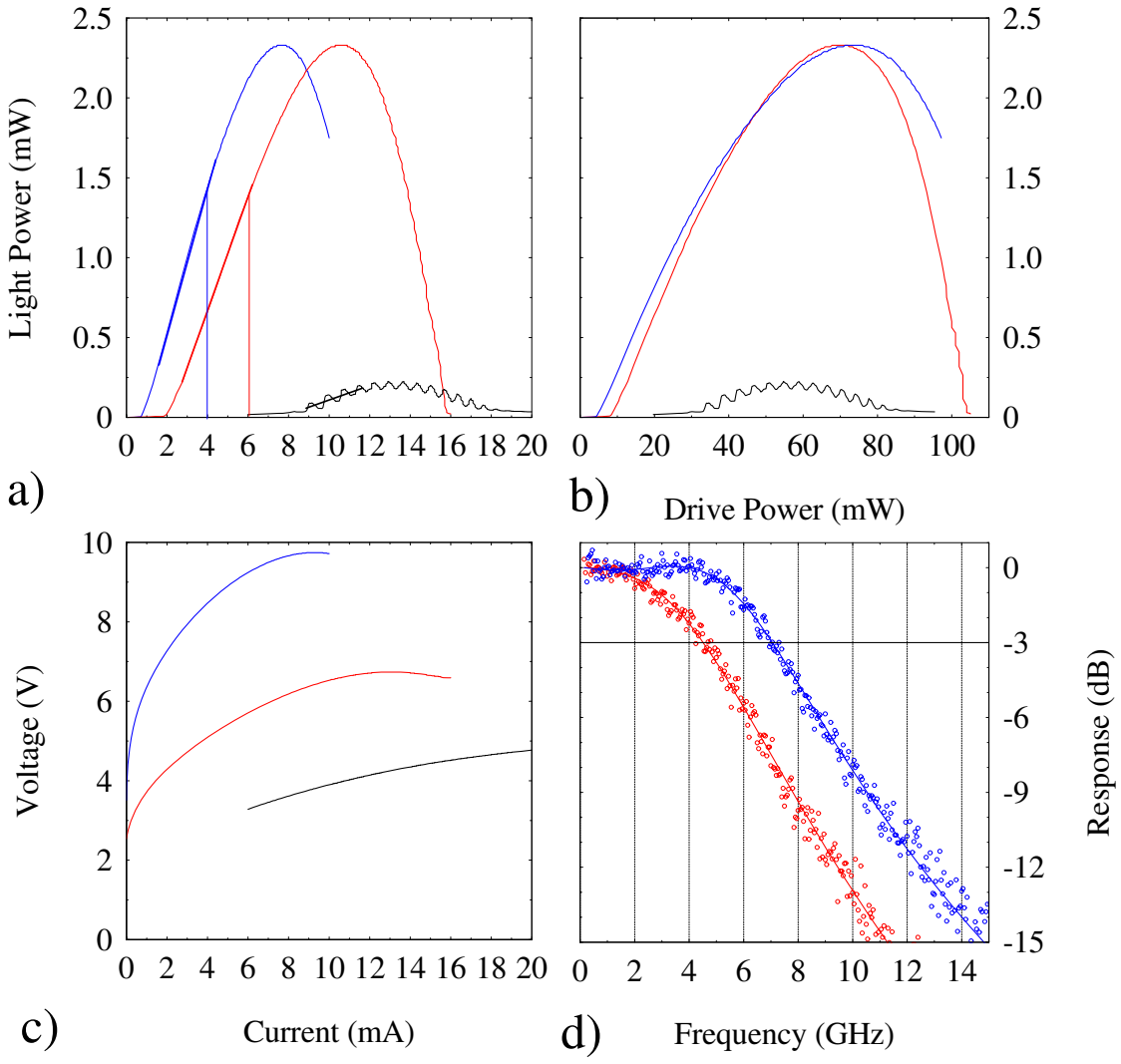


Figure C.7: Operating characteristics for 28 μm mesa 1- (black), 2- (red), and 3-stage (blue) BC VCSELs at a mount temperature of -50 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

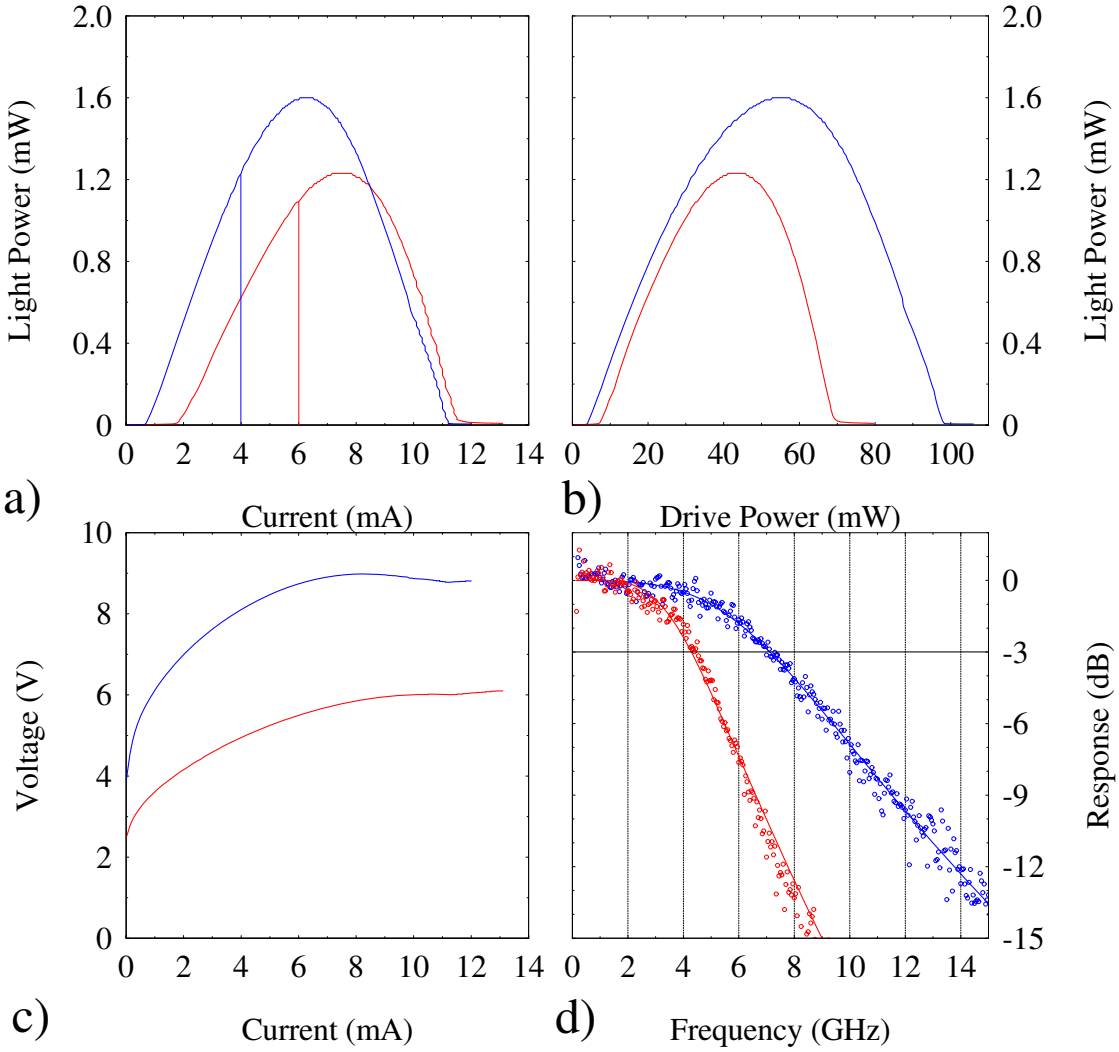


Figure C.8: Operating characteristics for 28 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of -25 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

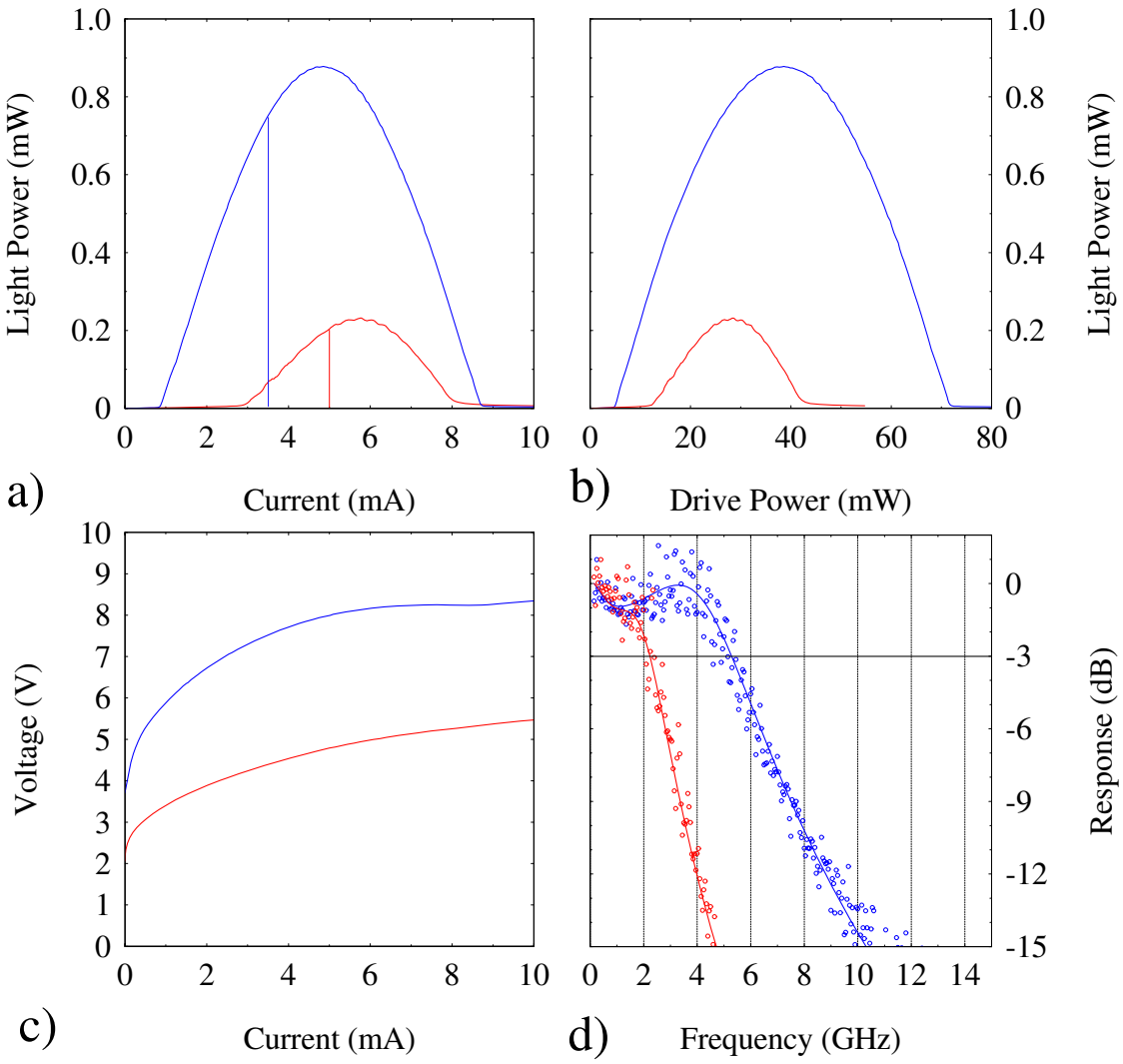


Figure C.9: Operating characteristics for 28 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of 0 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

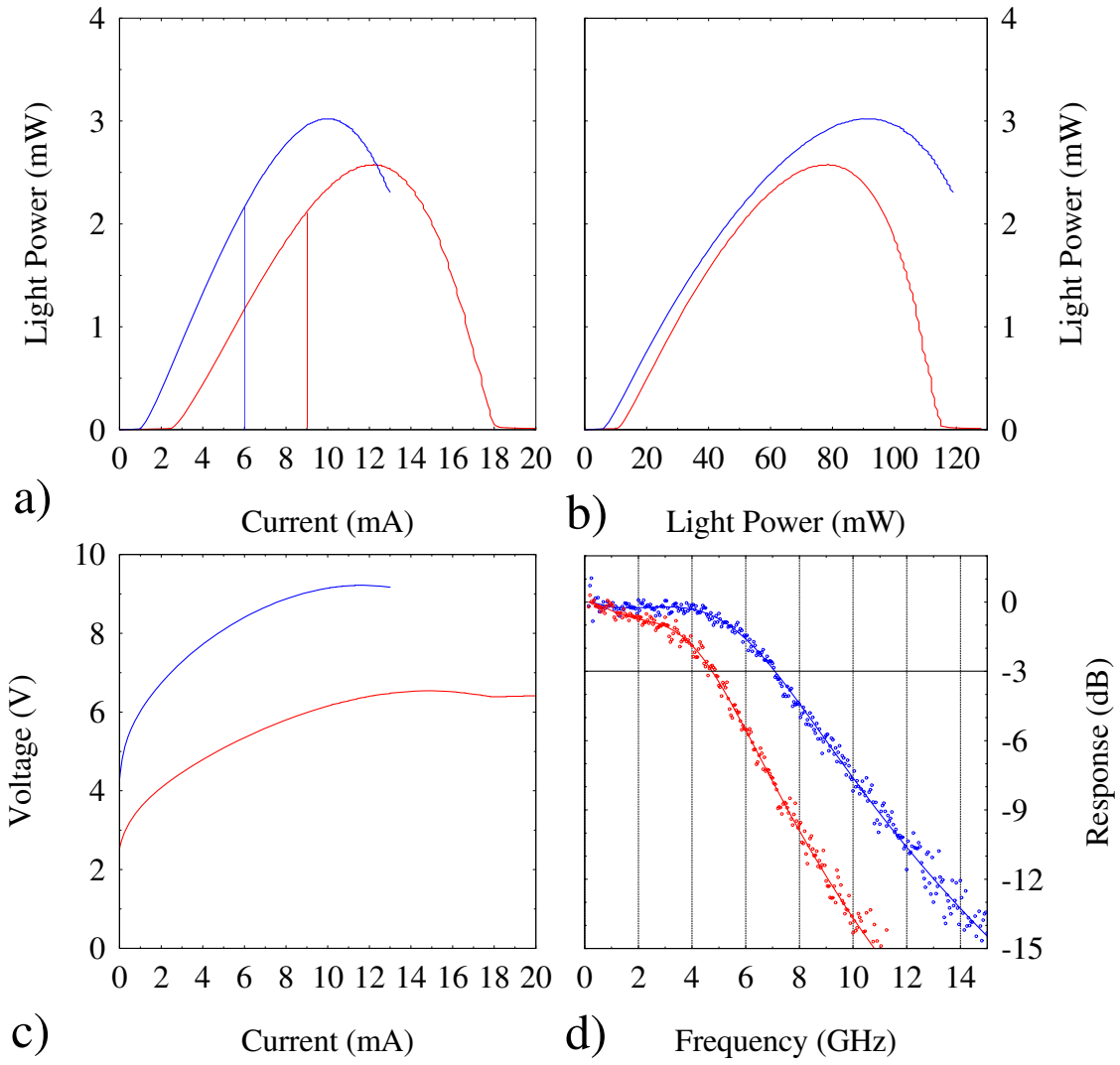


Figure C.10: Operating characteristics for 30 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of -50 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

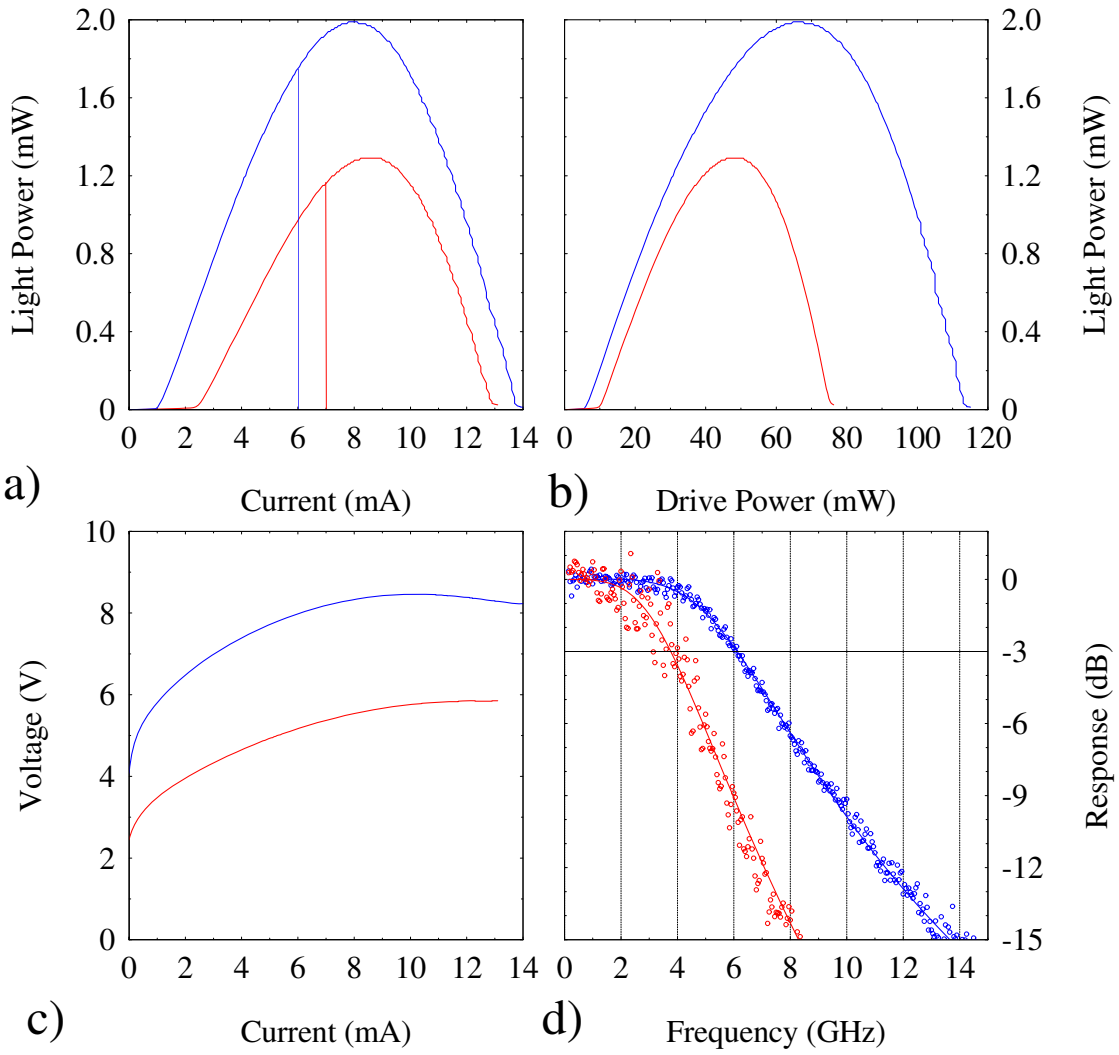


Figure C.11: Operating characteristics for 30 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of -25 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

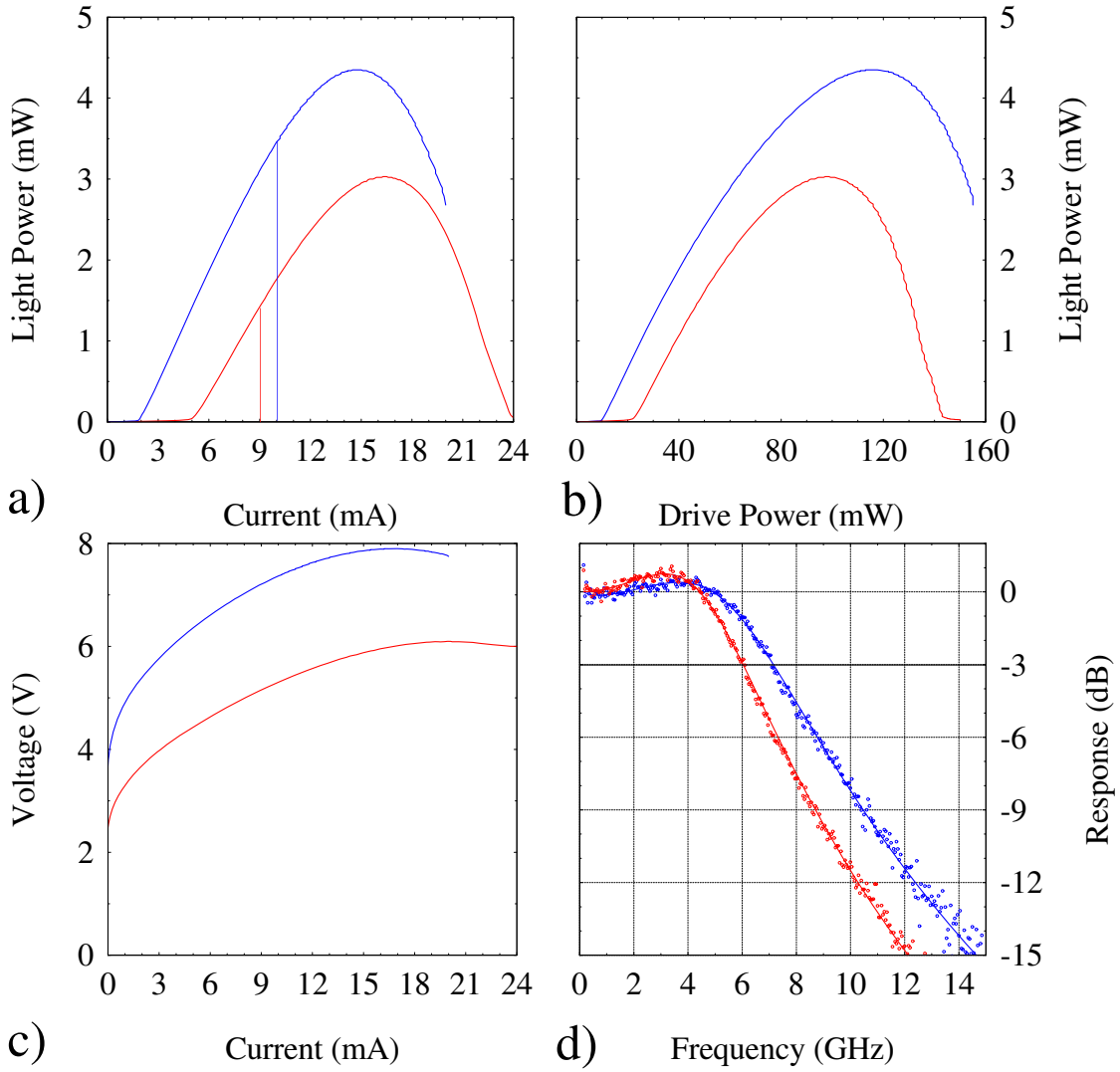


Figure C.12: Operating characteristics for 35 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of -50 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

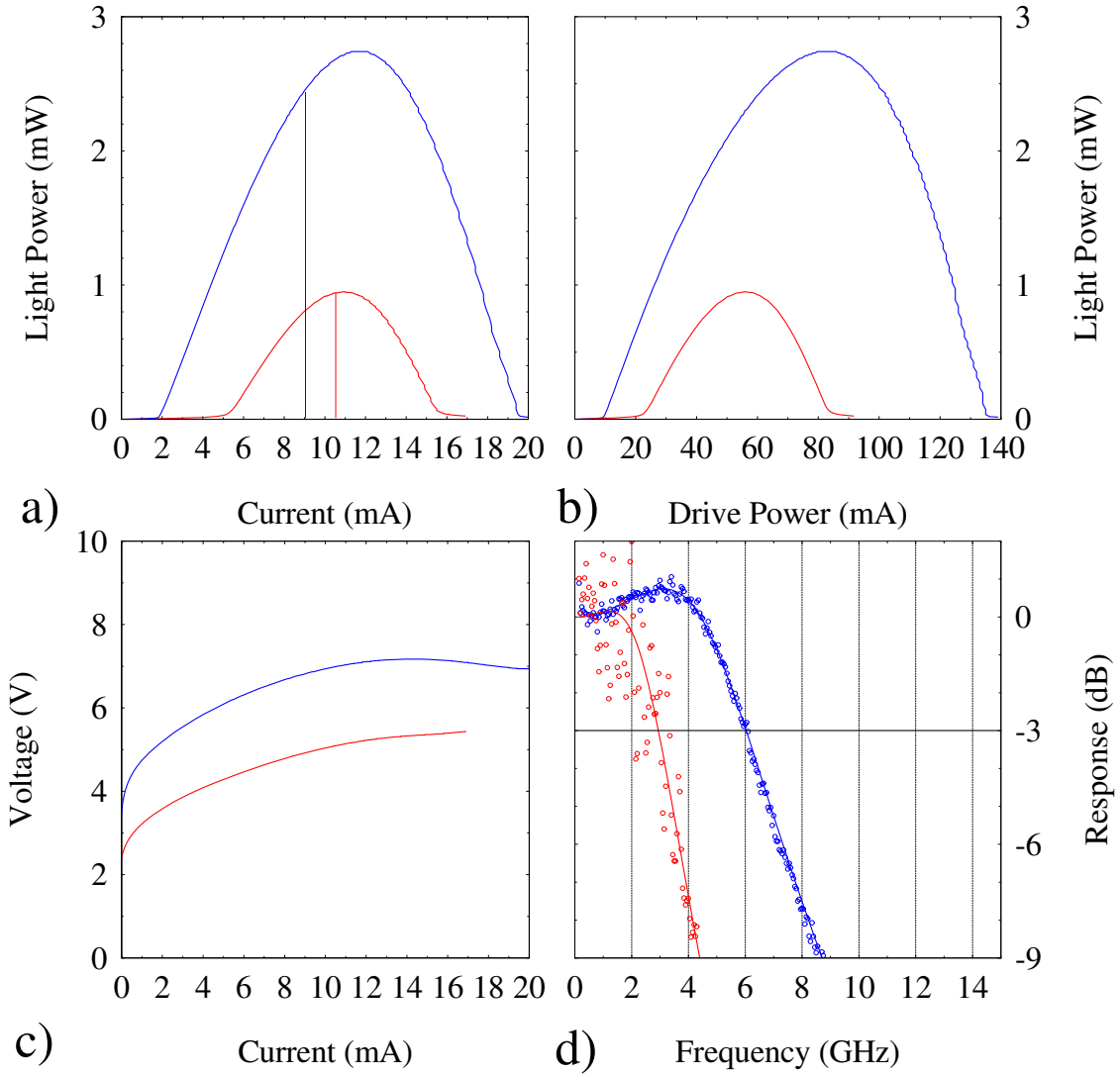


Figure C.13: Operating characteristics for 35 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of -25 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

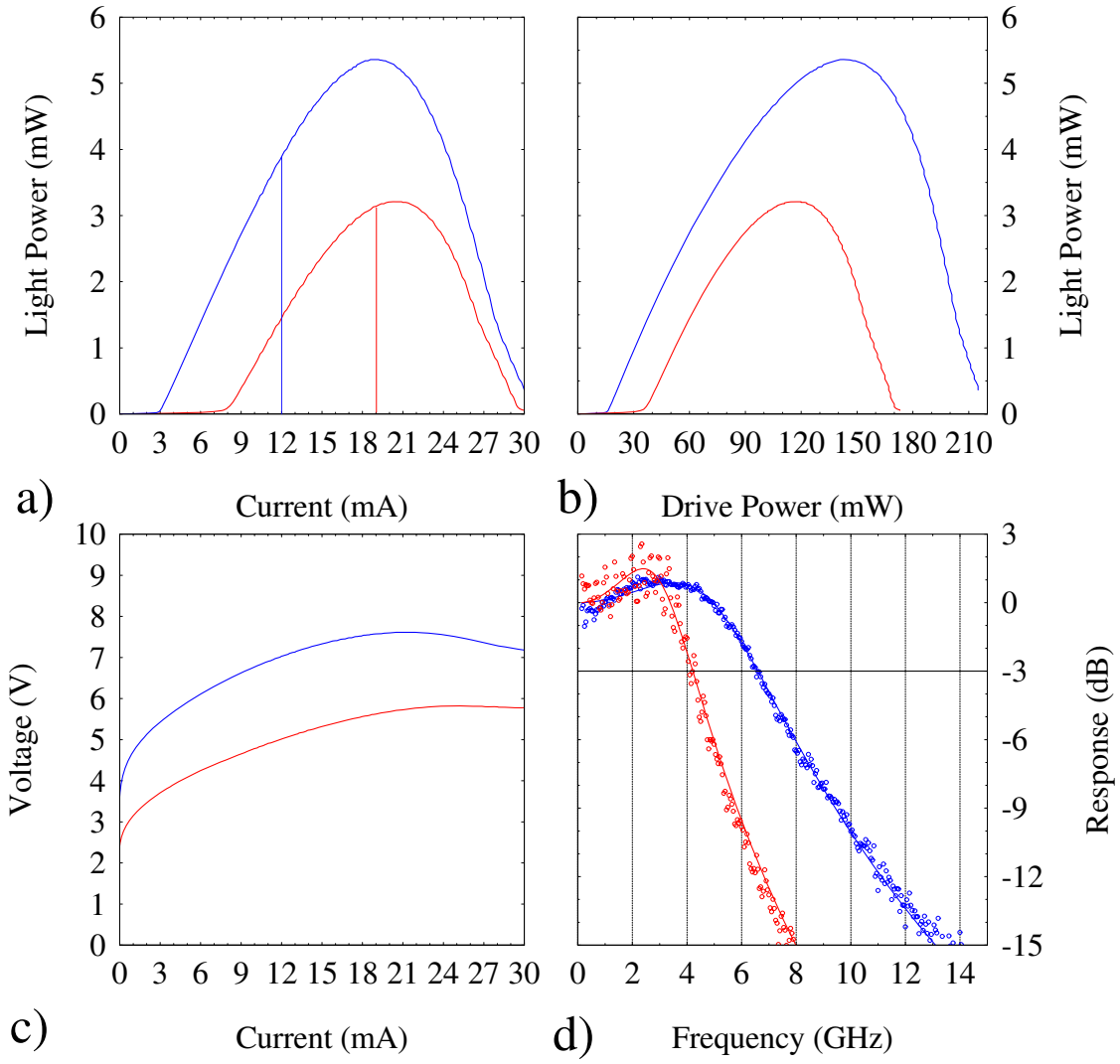


Figure C.14: Operating characteristics for 40 μm mesa 2- (red) and 3-stage (blue) BC VCSELs at a mount temperature of -50 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

Appendix D. Multiple Temperature Quad Charts

This appendix details device characterization by comparing individual 1-, 2-, and 3-stage BC VCSELs by mesa size as a function of temperature. The characterization is provided in a quad chart format for every mesa size with the a) chart illustrating the light power versus drive current (LI), the b) chart illustrating the light power versus drive power (LD), the c) chart illustrating the voltage versus drive current (VI), and the d) chart illustrating the frequency response. The color scheme is identical for all quad charts with mount temperatures of -50 °C (blue), -25 °C (red), 00 °C (black), and +25 °C (green). The vertical lines in the LI chart indicate the operating current the best performing frequency response shown in the frequency response chart in d).

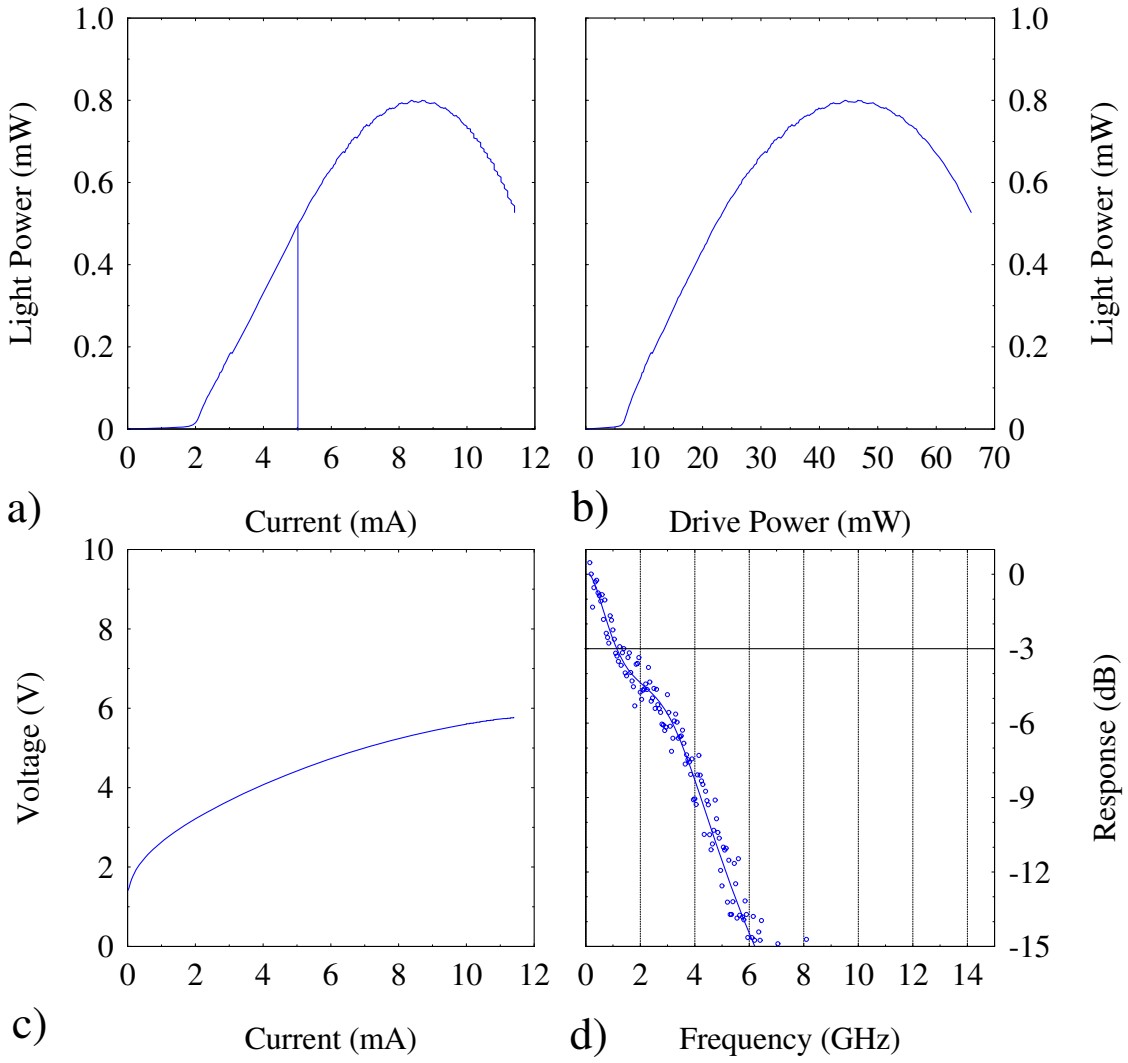


Figure D.1: Operating characteristics for 20 μm diameter mesa 1-stage BC VCSELs at a mount temperature of -50 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

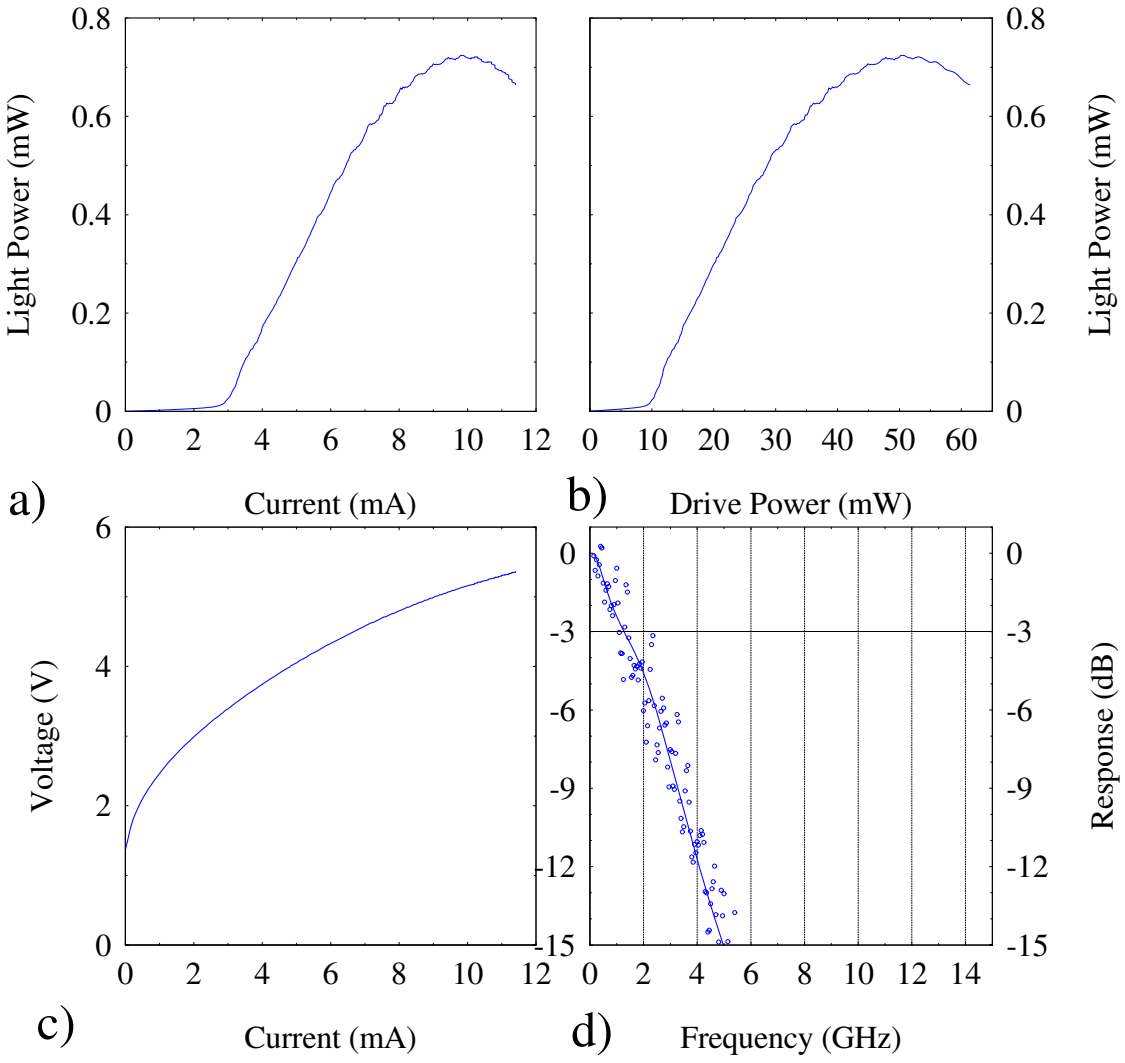


Figure D.2: Operating characteristics for 22 μm diameter mesa 1-stage BC VCSELs at a mount temperature of -50 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

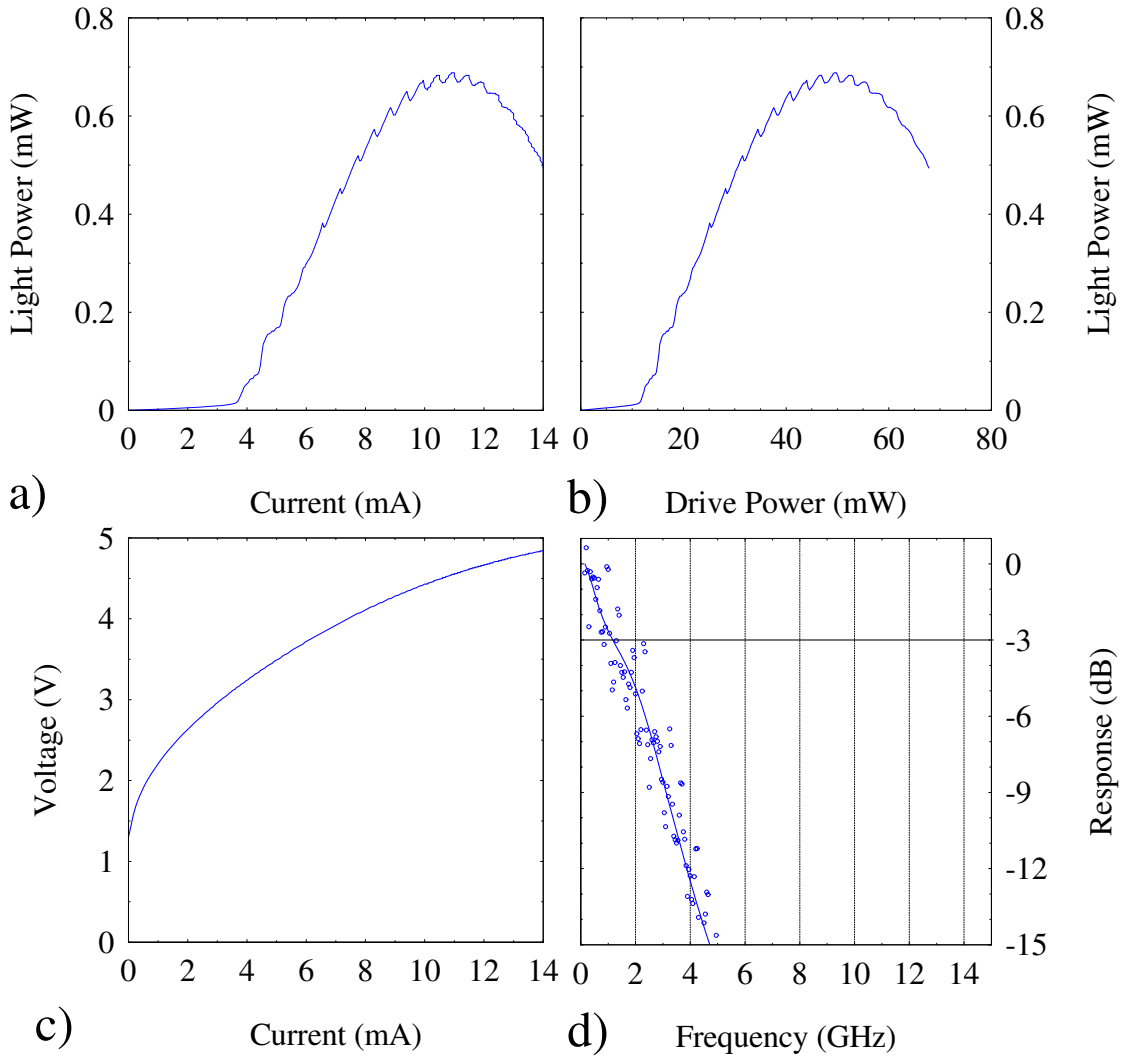


Figure D.3: Operating characteristics for 24 μm diameter mesa 1-stage BC VCSELs at a mount temperature of -50 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

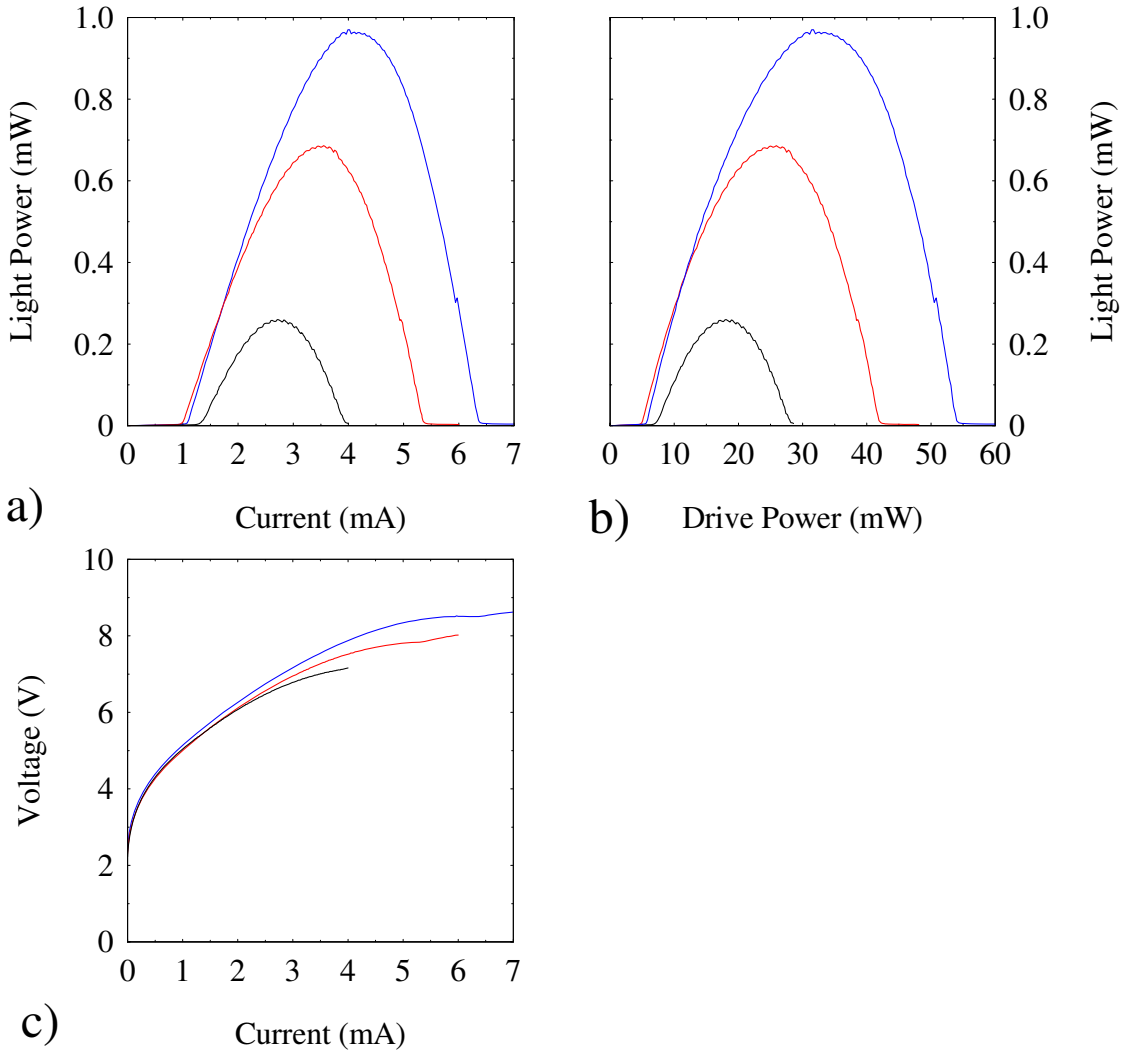


Figure D.4: Operating characteristics for 22 μm diameter mesa 2-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), and 00 °C (black). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

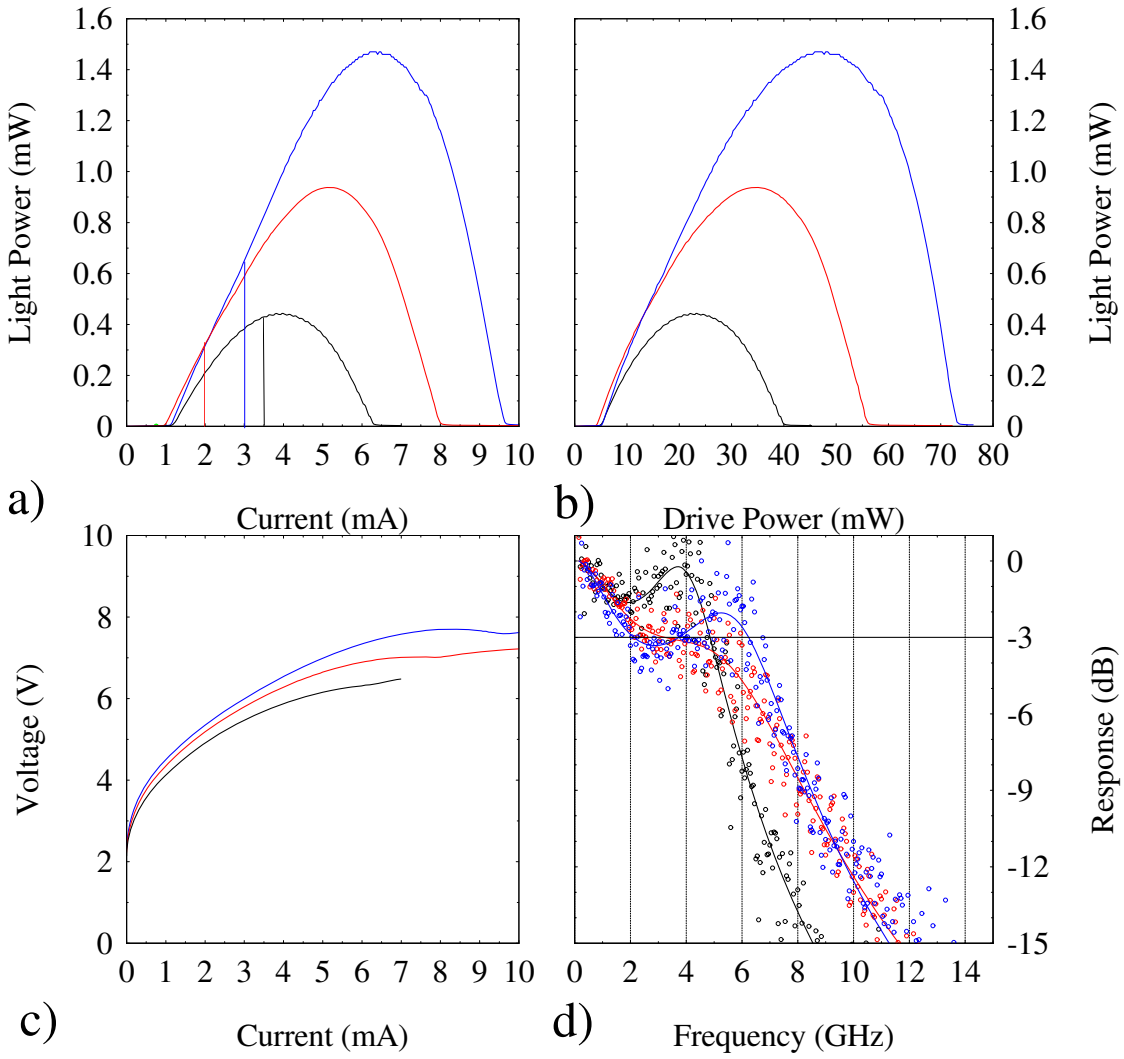


Figure D.5: Operating characteristics for 24 μm diameter mesa 2-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), and 00 °C (black). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

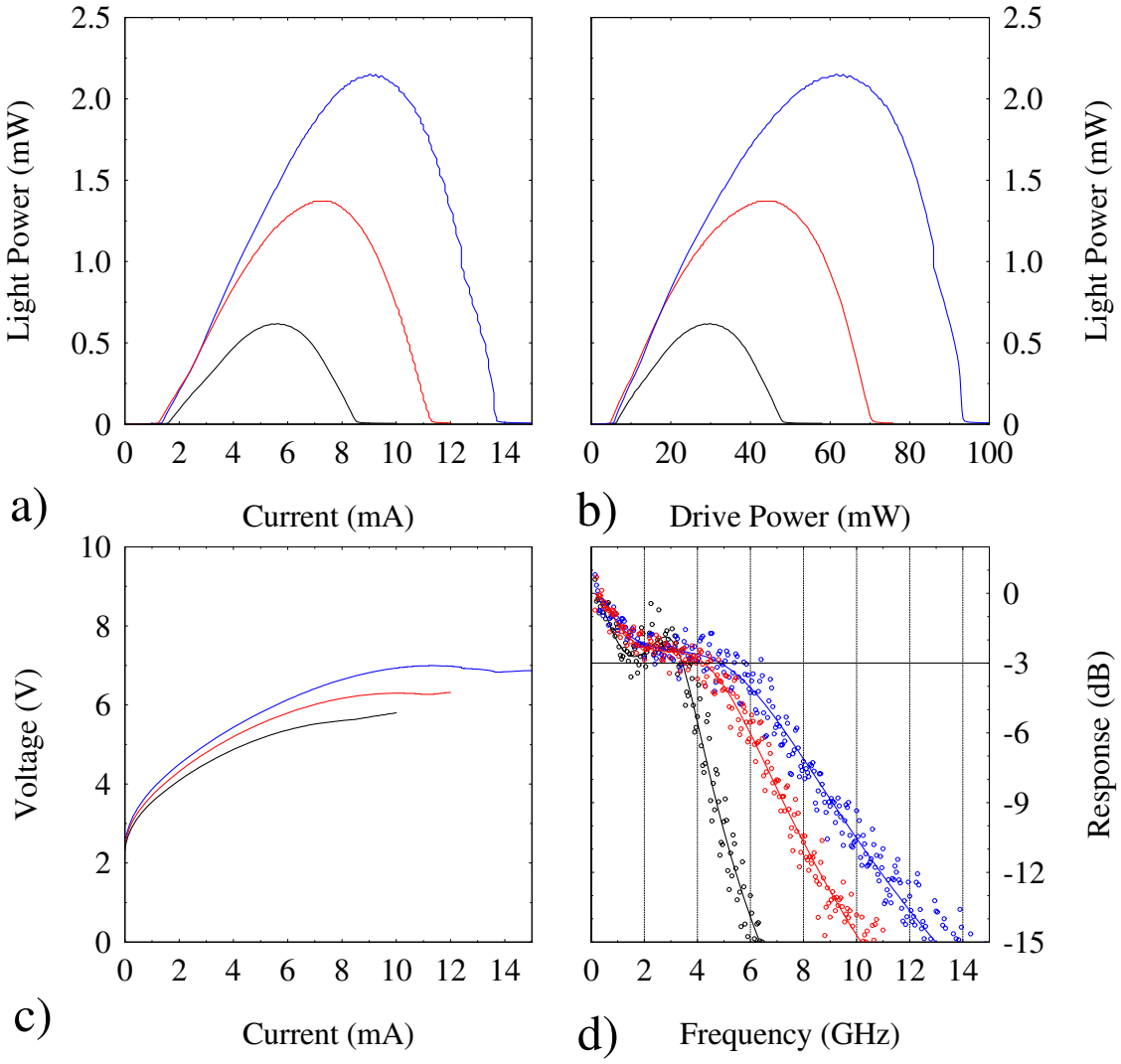


Figure D.6: Operating characteristics for 26 μm diameter mesa 2-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), and 00 °C (black). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

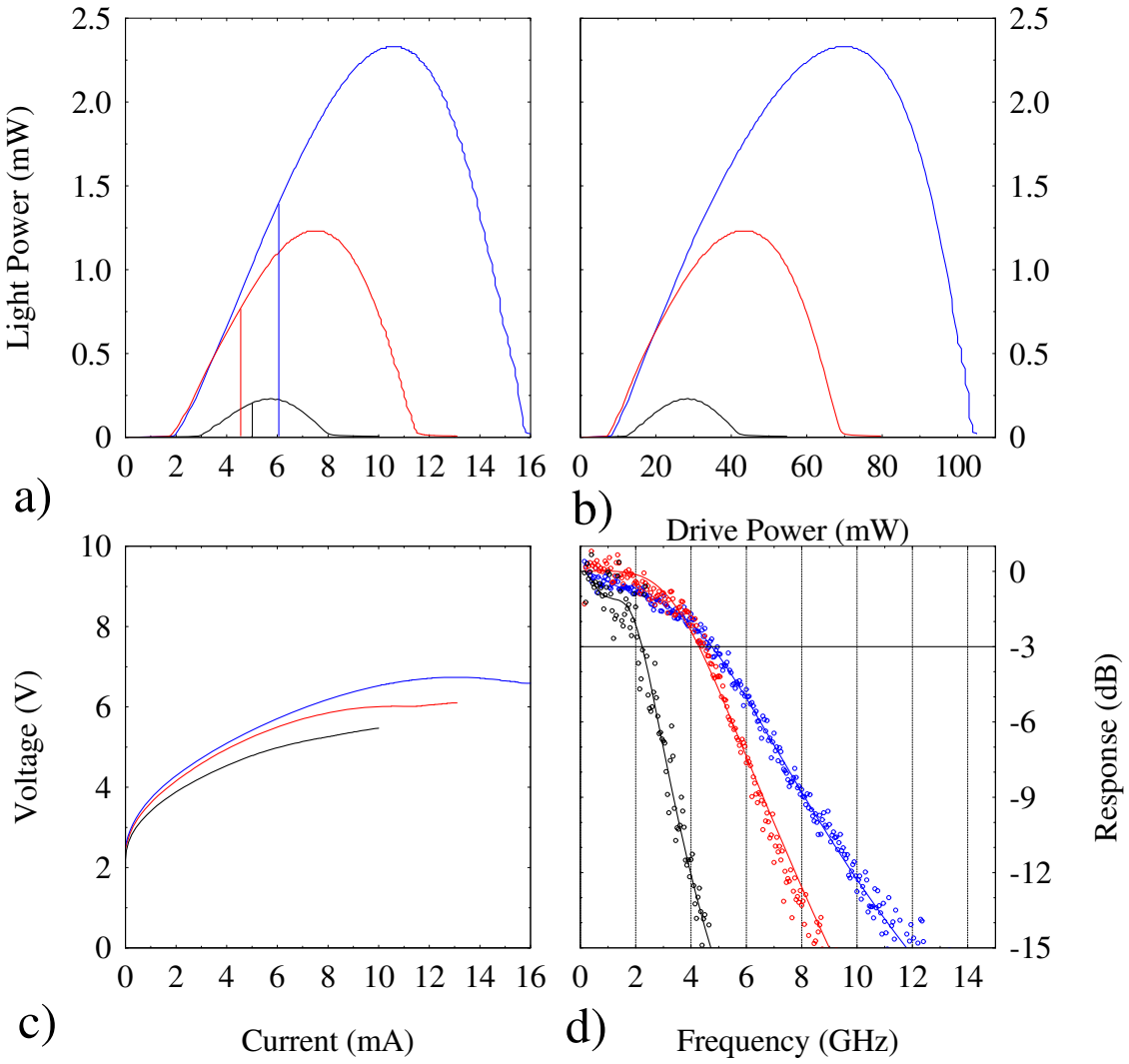


Figure D.7: Operating characteristics for 28 μm diameter mesa 2-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), and 00 °C (black). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

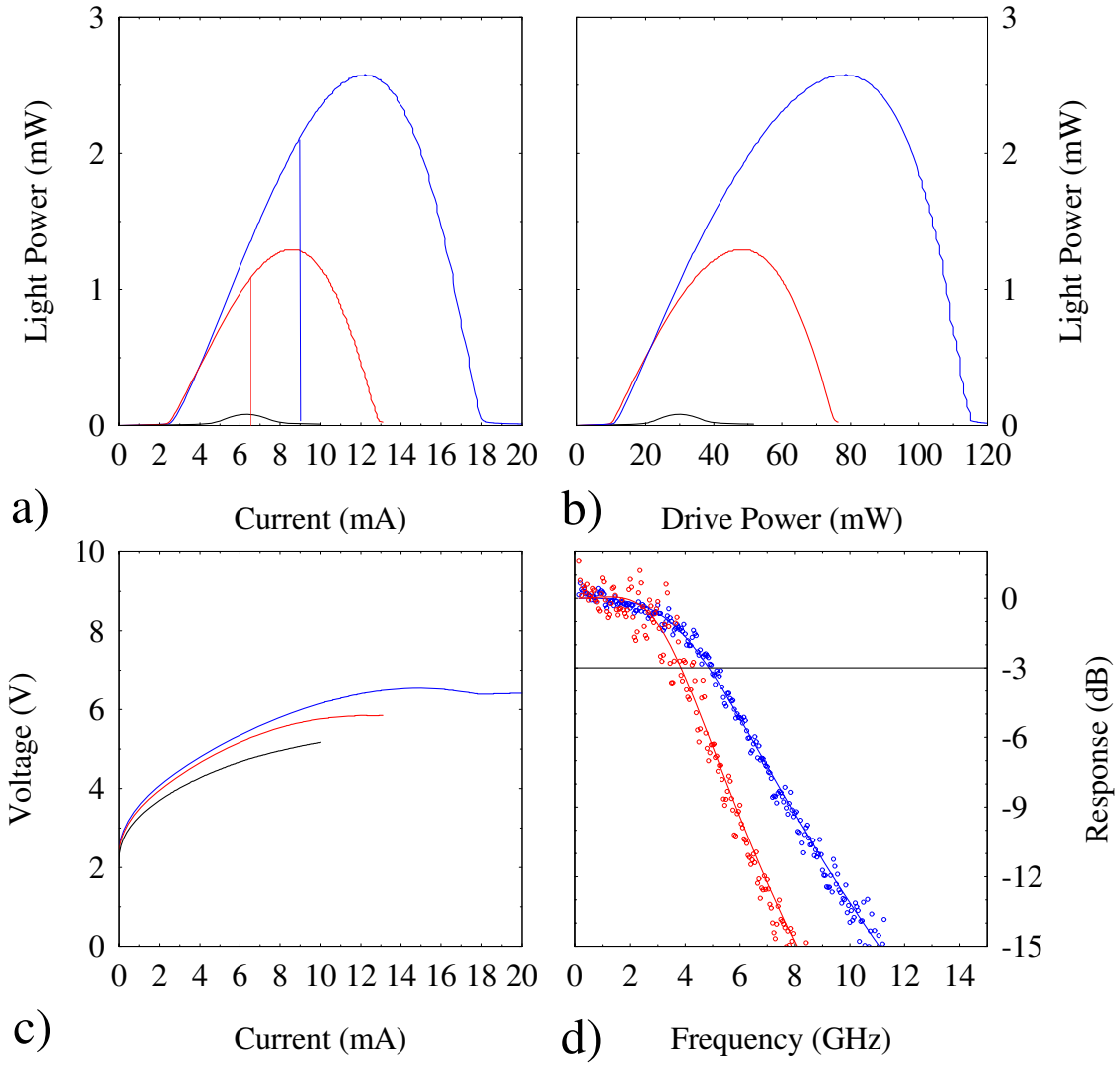


Figure D.8: Operating characteristics for 30 μm diameter mesa 2-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), and 00 °C (black). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

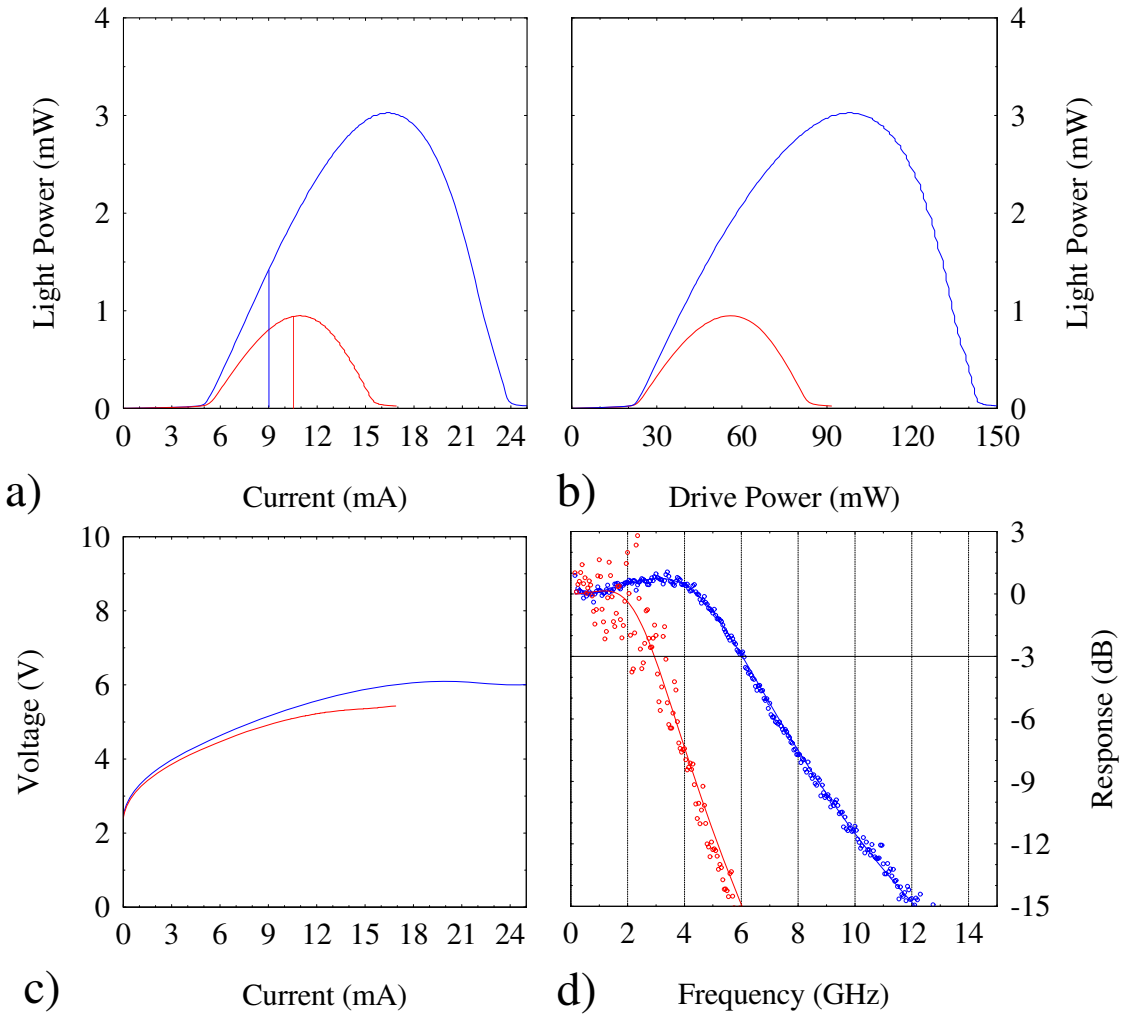


Figure D.9: Operating characteristics for 35 μm diameter mesa 2-stage BC VCSELs at mount temperatures of -50 °C (blue) and -25 °C. a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

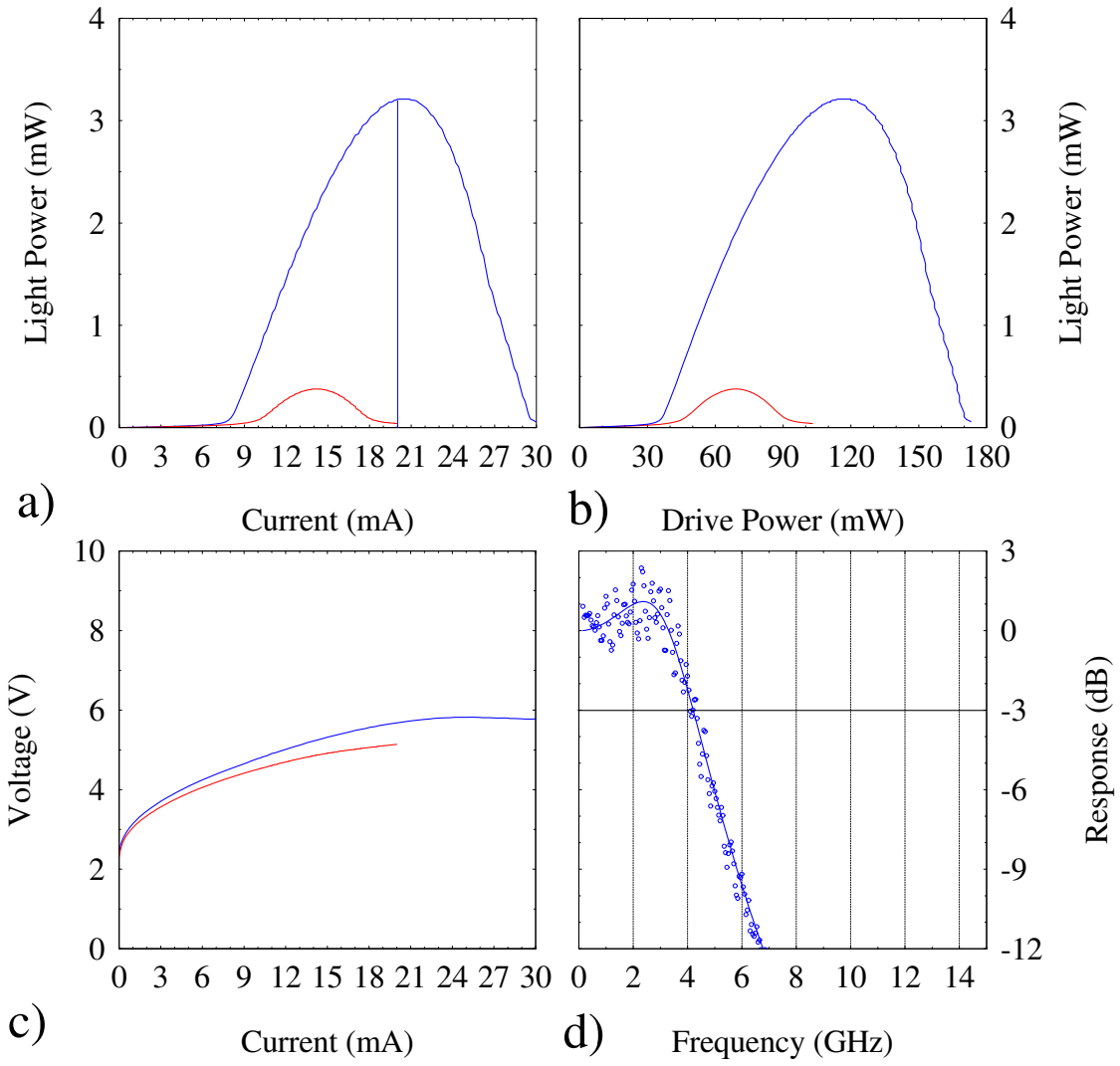


Figure D.10: Operating characteristics for 40 μm diameter mesa 2-stage BC VCSELs at mount temperatures of -50 °C (blue) and -25 °C (red). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

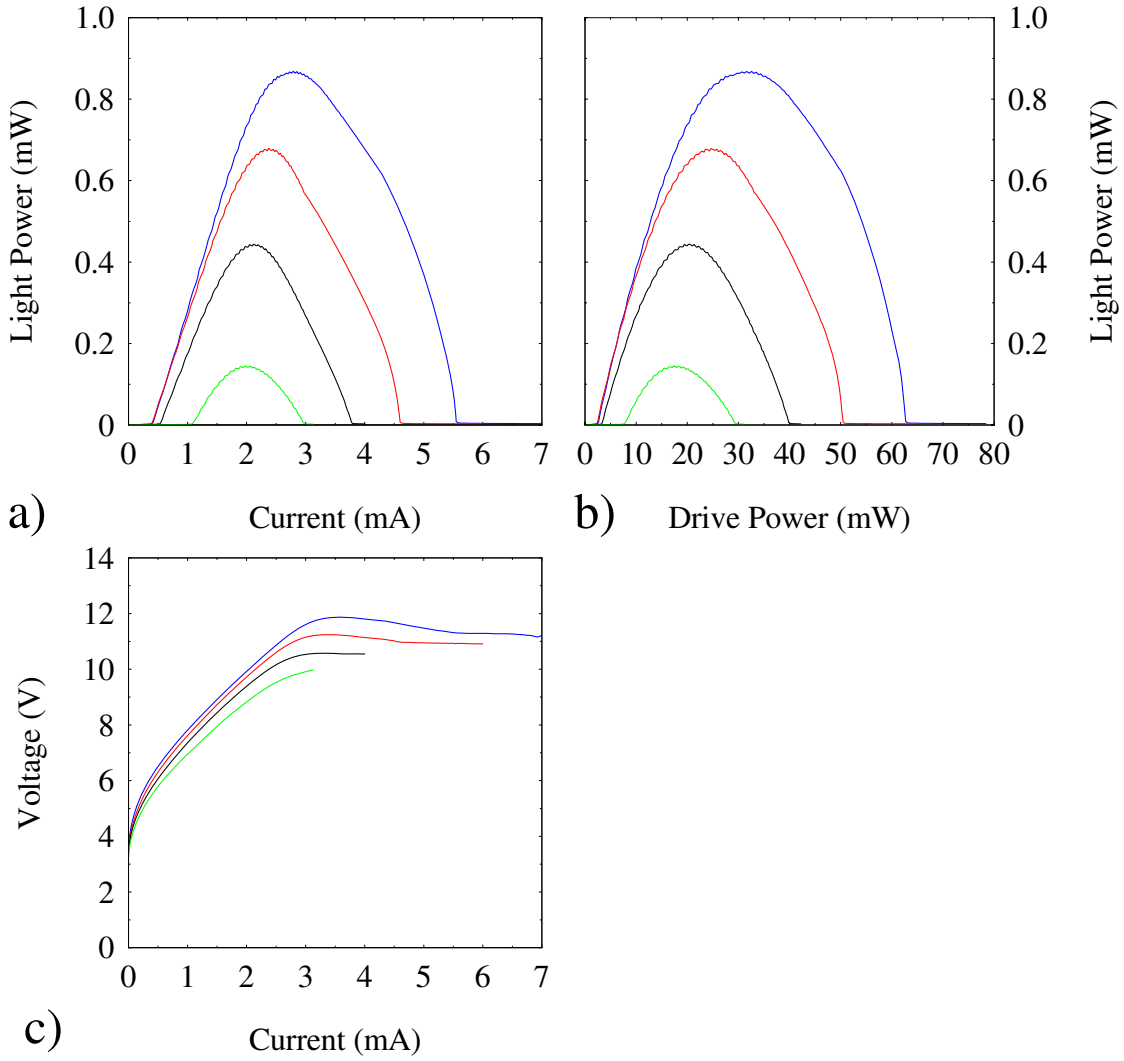


Figure D.11: Operating characteristics for 22 μm diameter mesa 3-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), 00 °C (black), and +25 °C (green). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

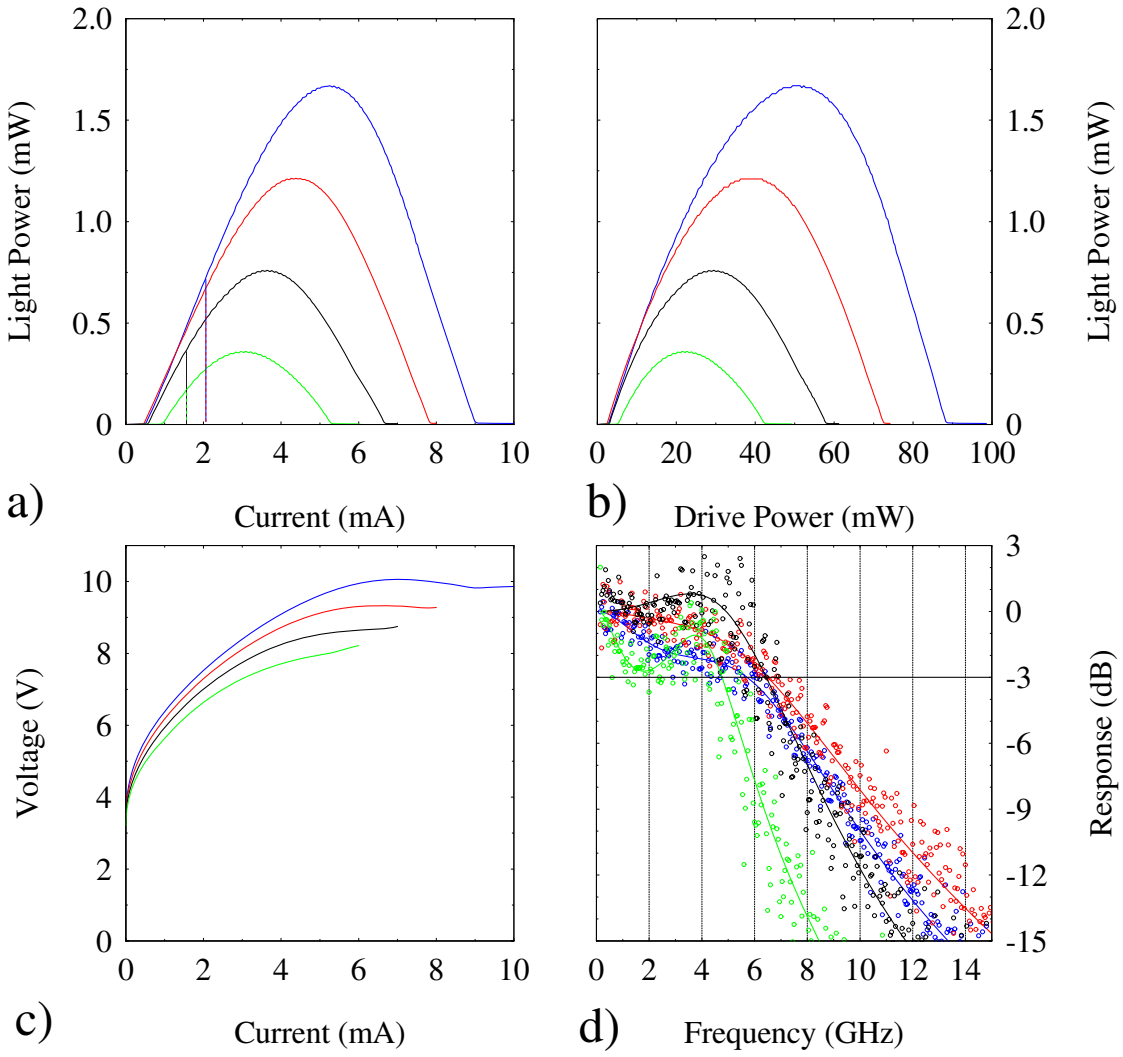


Figure D.12: Operating characteristics for 24 μm diameter mesa 3-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), 00 °C (black), and +25 °C (green). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

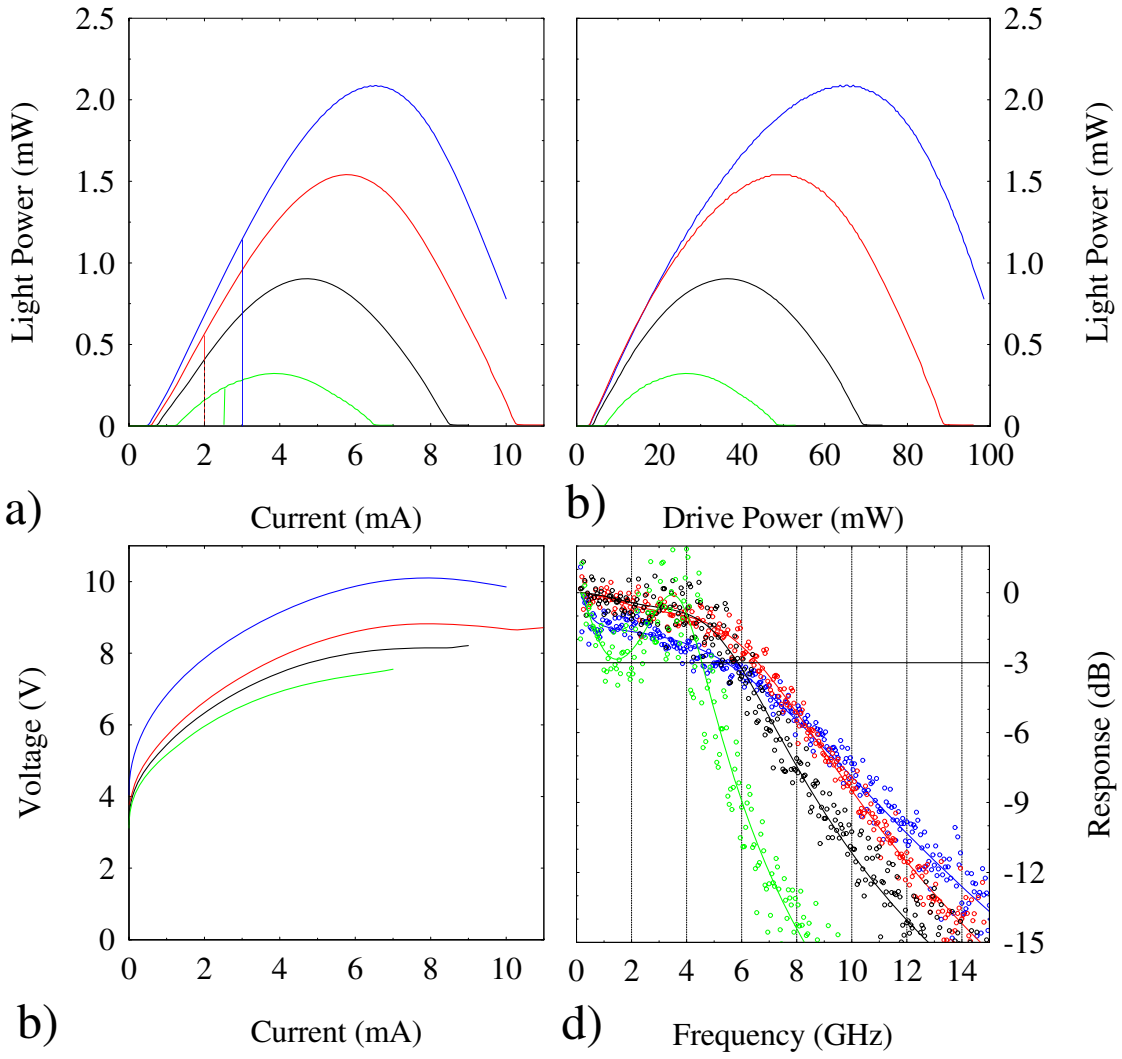


Figure D.13: Operating characteristics for 26 μm diameter mesa 3-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), 00 °C (black), and +25 °C (green). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

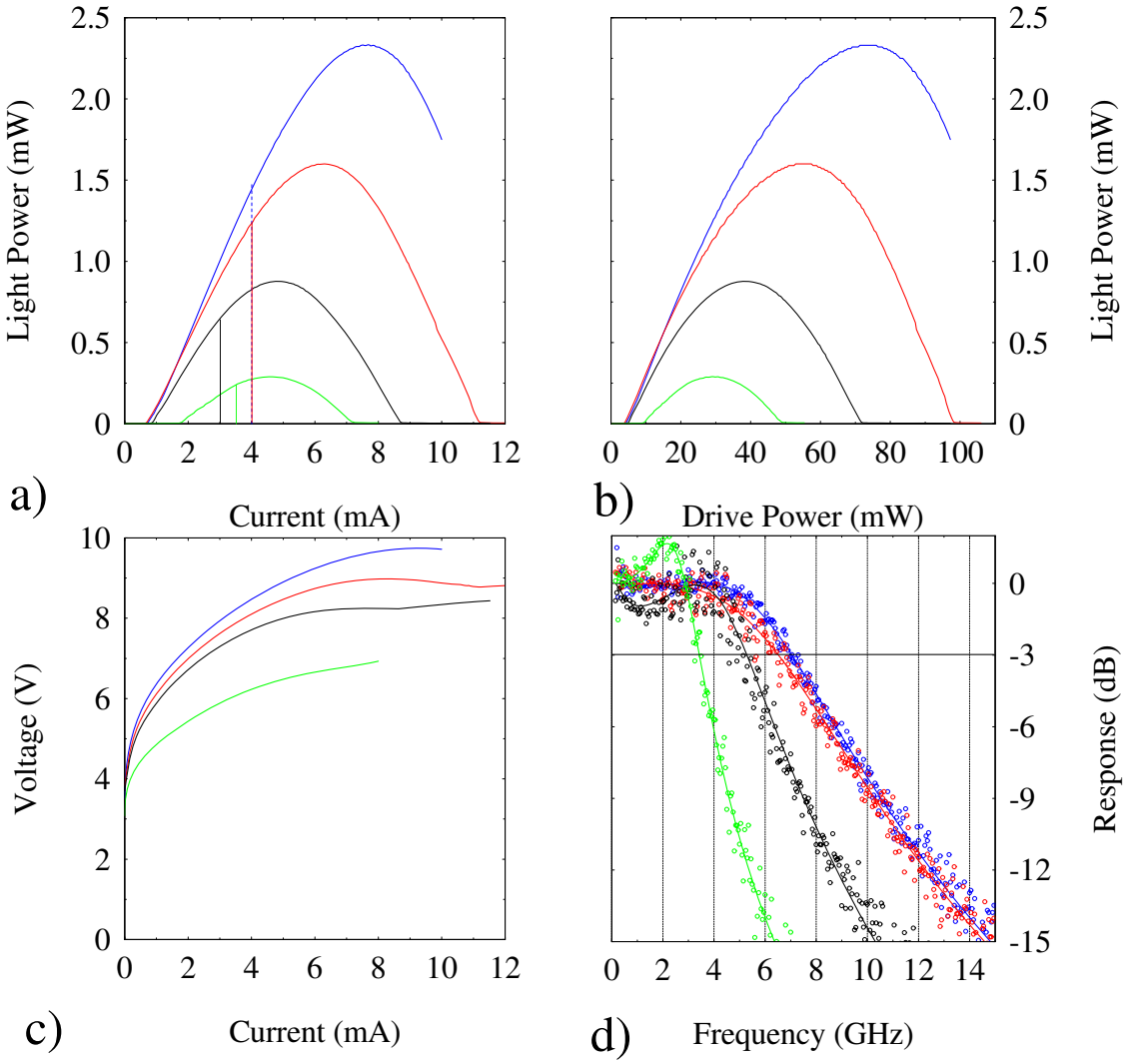


Figure D.14: Operating characteristics for 28 μm diameter mesa 3-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), 00 °C (black), and +25 °C (green). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

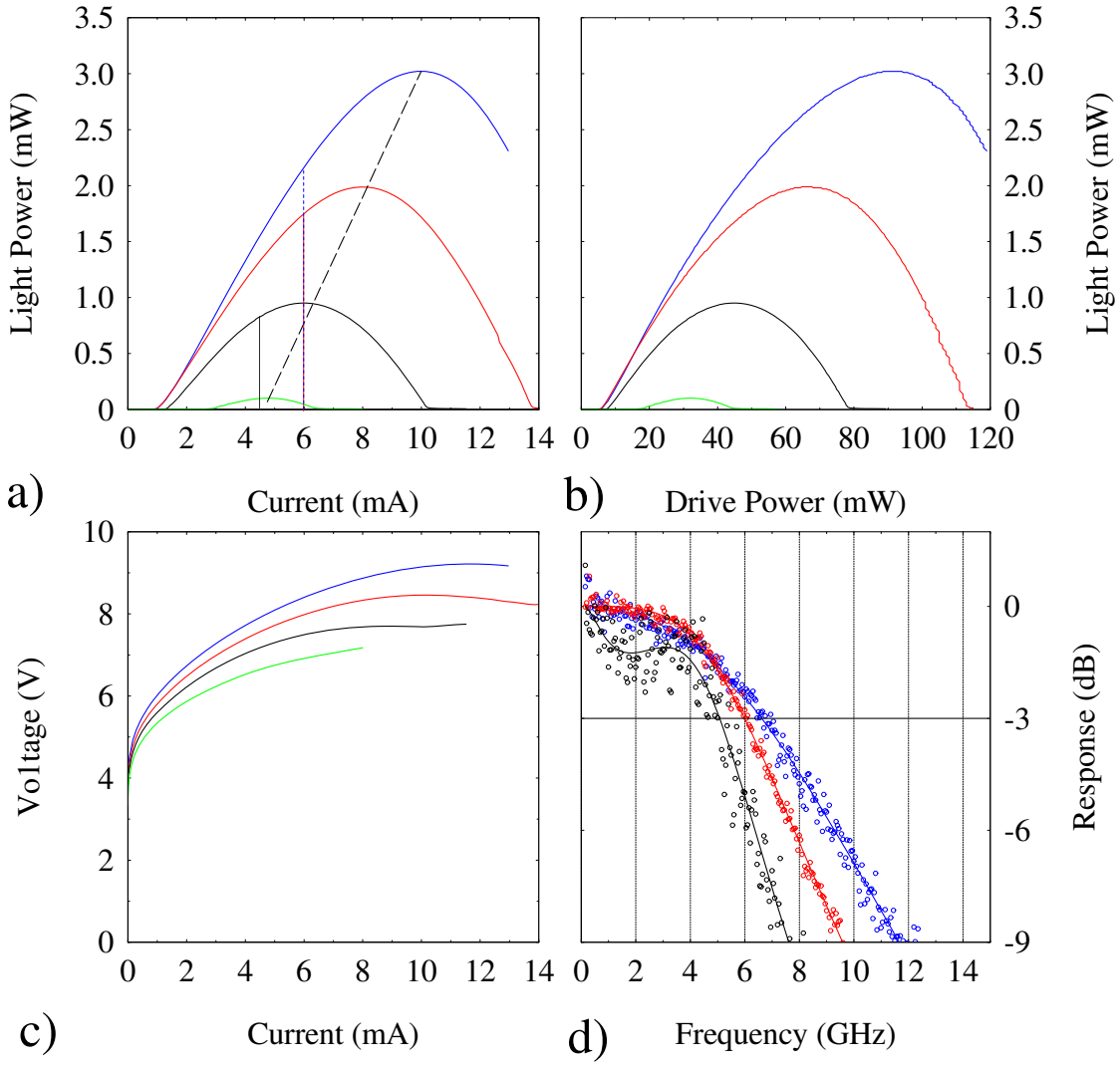


Figure D.15: Operating characteristics for 30 μm diameter mesa 3-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), 00 °C (black), and +25 °C (green). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

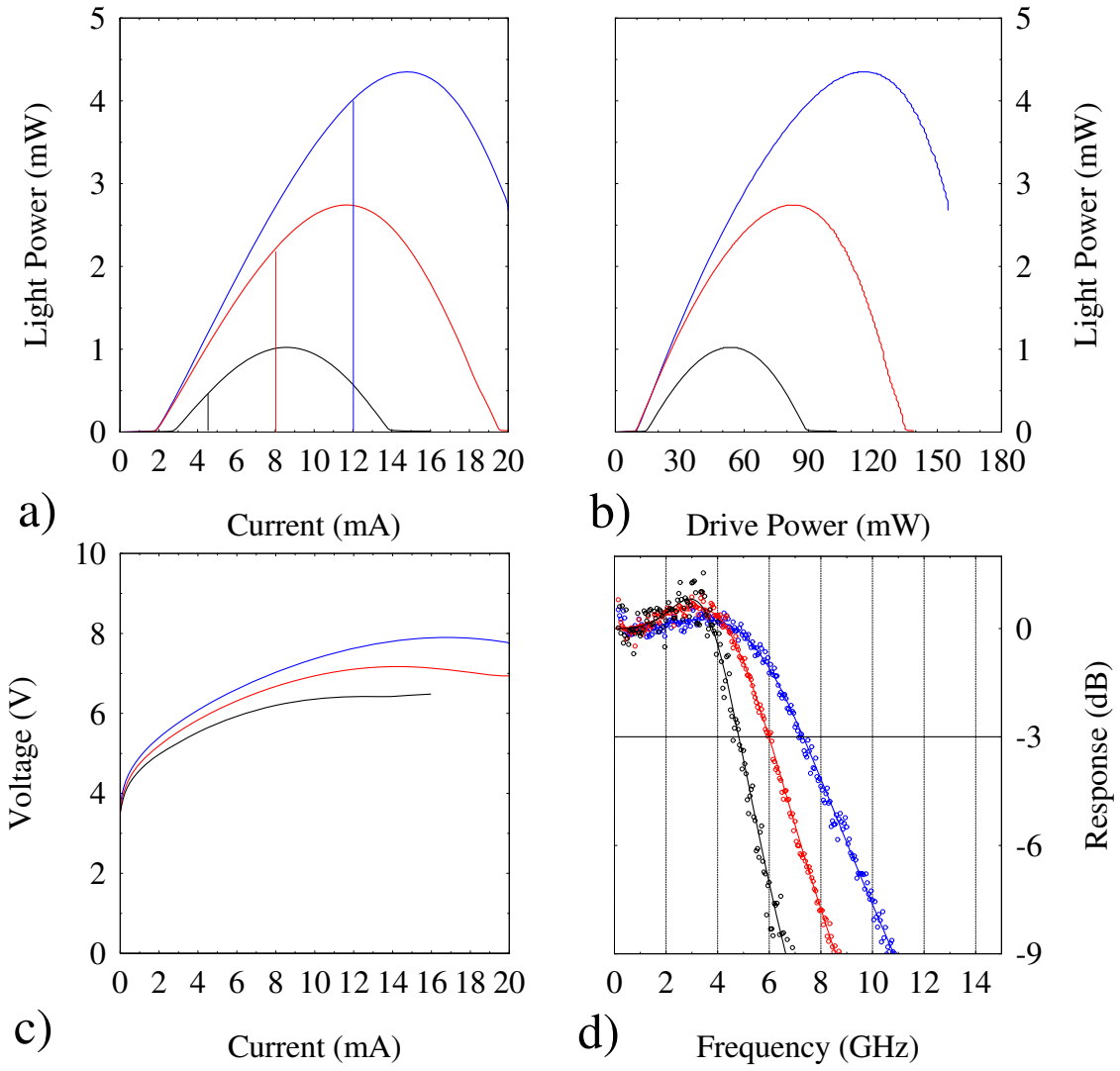


Figure D.16: Operating characteristics for 35 μm diameter mesa 3-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), and 00 °C (black). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

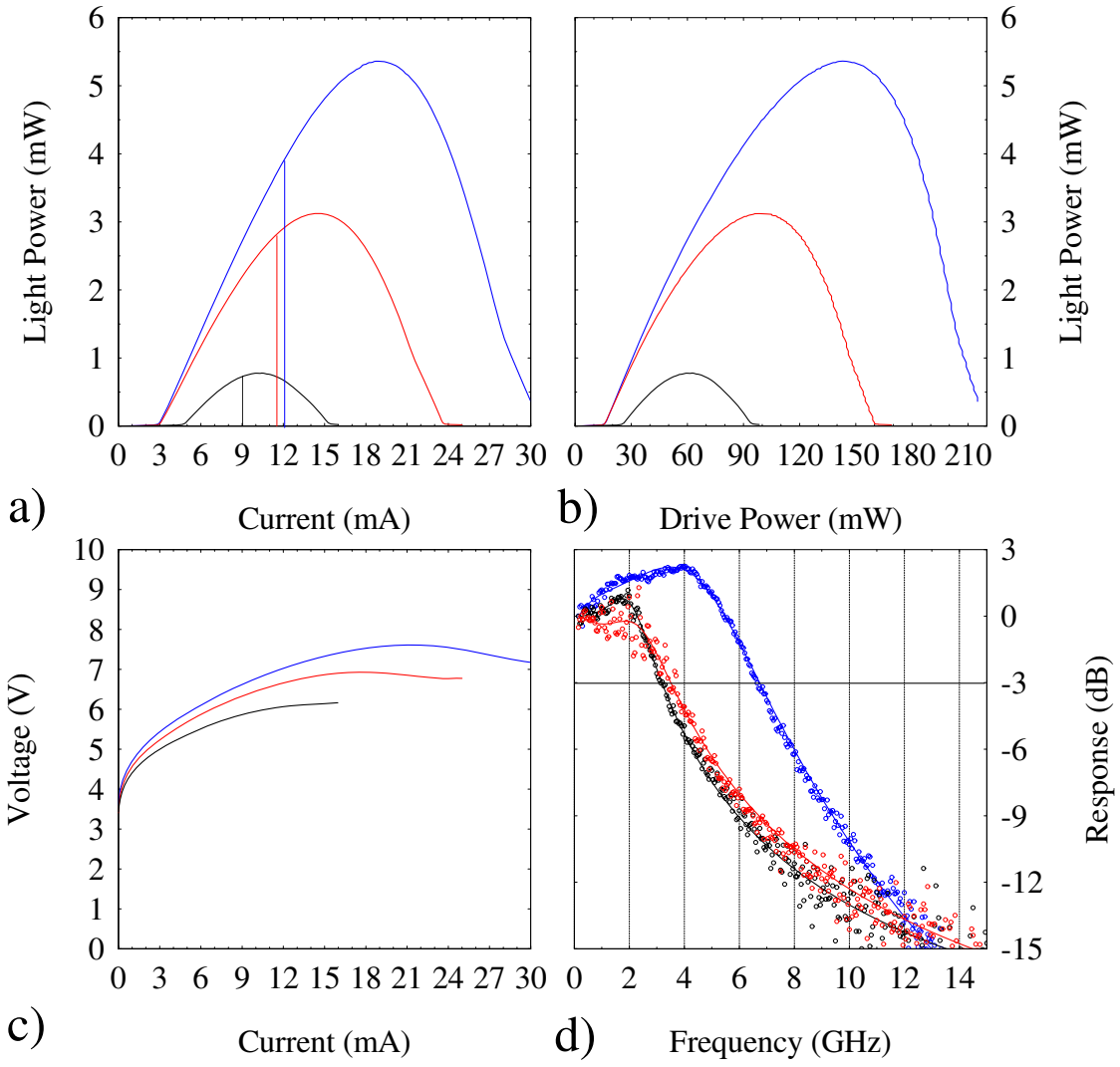


Figure D.17: Operating characteristics for 40 μm diameter mesa 3-stage BC VCSELs at mount temperatures of -50 °C (blue), -25 °C (red), and 00 °C (black). a) is the LI, b) is the LD, c) is the VI, and d) is the frequency response. The vertical lines in a) are the currents where the best frequency response characterization was obtained.

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14. ABSTRACT

The development and demonstration of bipolar cascade vertical cavity surface emitting lasers is presented. The systematic approach to designing, fabricating, and characterizing the critical tunnel junction, incorporating the tunnel junction into an edge emitting bipolar cascade laser, and finally the transition to a VCSEL structure is detailed. A novel approach prior to growing and characterizing BC VCSELs was to investigate bipolar cascade light emitting diodes which incorporate the microcavity designs and disentangles the VCSEL cavity effects from the microcavity.
The best performing p-doped oxide aperture microcavity design was then used as the microcavity for 1-, 2-, and 3-stage BC VCSELs. The high-frequency modulation characteristics of GaAs-based BC VCSELs operating at 980 nm with GaAs tunnel junctions and p-doped $Al_{0.98}Ga_{0.02}As$ oxide apertures have been measured and analyzed. Measured -3 dB laser output modulations of 4.5 GHz for 2-stage and 7.1 GHz for 3-stage devices in response to small-signal current injection at an operating temperature of -50 °C are reported and discussed.

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