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A Very Robust AlGaN/GaN HEMT Technology to High Forward Gate Bias and Current

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1. Introduction

There are recent reports stating that high negative gate bias causes the gates of GaN HEMTs to degrade. The signature of this degradation mechanism is an increase in gate leakage current [1–3]. Other reports state that forward gate current limits the survival times of GaN HEMTs, especially during RF operation [4, 5]. GaN HEMTs ($L_g = 0.7 \, \mu m$, $W_g = 2 \times 100 \, \mu m$) in [6] reached about 400 mA/mm forward gate current before burning out. The semi-insulating Fe-doped GaN of [6] was grown by MOCVD on sapphire substrates. Reference [7] specifically considered the effects of high positive gate bias (up to +6 V) on GaN HEMTs with gate-integrated field plates, $L_g = 0.25 \, \mu m$, and $W_g = 2 \times 25 \, \mu m$. By stepping $V_G$ from +0.5 V to +6 V in 0.5 V steps for 30 minutes per step, a reduction in $V_{Gon}$ ($V_G$ at a normalized gate current of 1 mA/mm) after 360 minutes was observed, accompanied by about a $10^4$ increase in gate leakage current and strong Ohmic gate behavior. The authors concluded that the large forward gate current and high temperature degraded the Schottky contact. Despite the reduction in $V_{Gon}$, [7] showed that there was little degradation in drain and source resistances and maximum drain current.

We show the results of stressing GaN HEMTs at extremely high gate current densities but for longer times and with more positive results. Despite the extremely high biases, the devices we tested survived well past the current density in [6] and were less conductive and with less $V_{Gon}$ degradation than those in [7]. Remarkably, it is noted that the devices we tested survived the stresses—contrary to conventional wisdom—with very little degradation in device drain current and voltage capability.

2. Experimental

We stressed four nominally identical AlGaN/GaN HEMTs. All four devices had the same structure which consisted of a semi-insulating SiC substrate [8], a 0.5 \mu m length optically defined gate with a gate-integrated field plate [8], and a source-connected field plate [9]. Gate width was $2 \times 50 \, \mu m$. The gate contained a nickel Schottky barrier and thick gold overlay for low gate resistance. The highly resistive GaN buffer was grown by OMVPE [8]. The AlGaN barrier
was undoped [8]. SiN, grown by PECVD, was used for passivation [8]. The gate-to-drain gap was greater than the gate-to-source gap [8].

The devices were tested on a Peltier thermal base plate in air. The power supplies used were Agilent models E5280A High-Power Source/Monitor Unit (SMU) Module (for the drain) and E5281A Medium-Power SMU Module (for the gate) in a model E5273A 2-Channel SMU.

We stressed the devices to define a safe operating area. An initially tested part (not shown) was stressed to $I_G = 260 \text{ mA/mm}$ at a base plate temperature of $T_{bp} = 35^\circ \text{C}$ without any discernable degradation, which provided the reference and motivation for this study. Based on this observation, a detailed study of gate robustness was conducted as described next. For this detailed study, the source and drain were wire-bonded and the gate was contacted by a needle probe. The following sequence was used at $T_{bp} = 45^\circ \text{C}$. The voltage-sweep and transfer-curve voltage ranges were divided into 201 linear, $\sim 35 \text{ ms}$ dwell steps ($\sim 7$ seconds total sweep time).

1. Characterize with a transfer curve ($V_G = -6 \text{ V}$ to $1 \text{ V}$ and $V_D = 10 \text{ V}$) before any stress and after each stress sweep (steps 2–6).
2. Sweep $V_G$ three times from 0 V to $+2.5 \text{ V}$ with $V_S = V_D = 0 \text{ V}$.
3. Sweep $V_G$ four times from 0 V to $+2.5 \text{ V}$ with $V_S = V_D = 0 \text{ V}$ and hold $V_G$ at $+2.5 \text{ V}$ for 1 minute.
4. Sweep $V_G$ from 0 V to $+3.0 \text{ V}$ with $V_S = V_D = 0 \text{ V}$ and hold $V_G$ at $+3.0 \text{ V}$ for 1 minute. Repeat at $+0.5 \text{ V}$ increments to $V_G = +6.5 \text{ V}$ ($I_G = 1.89 \text{ A/mm}$).
5. Sweep $V_G$ from 0 V to $+6.0 \text{ V}$ with $V_S = V_D = 0 \text{ V}$ and hold $V_G$ at $+6.0 \text{ V}$ for 30 minutes.
6. Repeat step 5 with 30-minute, 150-minute, 120-minute, and 1-hour holding times, respectively, at $V_G = +6.0 \text{ V}$ ($I_G \approx 1.82 \text{ A/mm}$). After the last hold, the device was in a small-bias state ($I_G = 300 \mu\text{A/mm}$, $V_S = V_D = 0 \text{ V}$) for two days due to the gate contact needle probe coming loose.

In summary, the test lasted more than 17.5 hours at $V_G = +6.0 \text{ V}$ in addition to 1 minute at $V_G = +6.5 \text{ V}$.

### 3. Results and Discussion

Results from one of the tested devices are described in the following. In summary, the device survived for $>17.5$ hours the stress of biasing at $V_G = +6.0 \text{ V}$ and $I_G \geq 1820 \text{ mA/mm}$ forward gate current (see Figure 2), which is a current density of $>360 \text{ kA/cm}^2$ and $>10.9 \text{ W/mm}$ power through the gate. $I_{D_{\text{max}}}$ (defined as drain current at $V_G = 1 \text{ V}$ and $V_D = 10 \text{ V}$) degraded slightly and saturated over stress duration (see Figure 1). After 210 minutes of stress, degradation in the ideality of $I_G/V_G$ was observed at low currents (see the upper left inset of Figure 2), although it is noted that this ideality degradation did not significantly impact the current handling capability and breakdown voltage capability of the device.

The forward gate current values from our tested devices were far more than the value of $400 \text{ mA/mm}$ ($57 \text{ kA/cm}^2$) reported in [6] that destroyed the particular GaN HEMTs tested in that report. The devices tested in this report were also less conductive at high gate bias [1.63 A/mm, $326 \text{ kA/cm}^2$ at $V_G = +5 \text{ V}$] compared to those of [7], wherein the forward gate current was reported to be $2 \text{ A/mm}$ ($800 \text{ kA/cm}^2$) at $V_G = +5 \text{ V}$. We note that these comparisons are to devices with different gate lengths, contact and sheet resistances, and source-to-gate-to-drain gaps, although the results made strictly refers the robustness of the Schottky gate which is less sensitive to these differences.

Figure 1 shows the transfer curves and associated gate current in absolute value and transconductance of the device throughout stressing. Black lines show step 1 (initial) and the last repeat of step 2; red lines show the last repeat of step 3 and results of step 4; finally, green lines show steps 5–6. Initial slight improvement in gate current (trapping or burn-in behavior likely) gives way to degradation. The transfer curves exhibit a degradation trend with a saturation apparent after the first 30-minute holding time, much like a transient burn-in effect. Two separate causes—resulting in quick degradation in the short term and slow degradation in the long term—appear responsible for the electrical changes observed during exposure to bias. The gate current increases in a different fashion, with a decreased rate of change—leading to possible saturation—after the first several hours of stress. There was little drain current degradation at the tested current density—a 6.1% reduction, comparing the prestress $I_{D_{\text{max}}} = 787 \text{ mA/mm}$ to the poststress $I_{D_{\text{max}}} = 739 \text{ mA/mm}$. In addition, there was only a 0.1 V positive shift in threshold voltage.

Figure 2 shows the device’s gate diode curves during the stress sweep from $V_G = 0 \text{ V}$ to $+2.5 \text{ V} \leq V_G \leq +6.5 \text{ V}$ (steps 2–6). During the first few sweeps, the gate current improved. After this, excess leakage at low gate bias appeared (see upper left inset), then the gate current increased with stress time and saturated. Despite the ideality degradation, the breakdown voltage remained above 200 V (based on satisfying the nominal 1 mA/mm industry criterion for breakdown). If there is any change in $V_{\text{Gen}}$, it is slight and masked by other effects. In contrast, [7] observed a noticeable change in $V_{\text{Gen}}$ of $-0.5 \text{ V}$ in significantly shorter stress time.

There are insufficient details in [6, 7] to adequately compare and contrast those structures and the present structure. However, technology maturity, gate metal stack differences, and the source-connected field plate in the present technology are possible factors for the observed improvements. Reference [10] provides a physical explanation why positive gate bias and current may not be as damaging to GaN HEMTs as conventional wisdom dictated. Reference [10] also provides an example of observations that do not conform to expectations for thermally induced degradation: transconductance degraded more for a semi-ON state than for a higher-power ON state.

The high forward gate current seen in this testing would have caused significant degradation or failure in earlier vintage GaN HEMTs. The tested GaN HEMTs exhibited the ability to withstand nearly constant high forward gate stress and...
demonstrated a high level of allowable forward gate stress. The drain current failure criterion in [9] was $-10\% I_{DS}$, the nominal industry gate leakage failure criterion is 1 mA/mm. Neither failure criterion was reached in the characterizations of the present testing (see Figure 1). Although the gate leakage increased more than two orders of magnitude (see Figure 1(b)), $I_{D\text{max}}$, $V_{G\text{on}}$, and the breakdown voltage were not significantly affected. Of course, the maximum allowable degradation in any particular parameter depends on the specific application.

We should clarify that we do not anticipate continuous long-term bias in real-world operation at the high $V_G$ conditions we have tested and are not stating that this has been shown to be practical. Instead, we showed that brief excursions, or short-term operation, up to $V_G = +6.5\, \text{V}$ may be feasible. Based on the stress time endured for this testing, such excursions would not be catastrophic.

To estimate device lifetime due to high forward gate stress, an appropriate accelerant and acceleration model would need to be determined (since testing at use conditions is impractical) through additional testing and analysis. In [3], the authors state that gate degradation due to high reverse gate bias is weakly dependent on temperature and strongly dependent on gate voltage. Gate voltage may also be an accelerator for forward gate stress. Physical failure analysis would also be required to understand the degradation due to high forward gate stress.

4. Conclusion

The mere survival of the device tested at $I_G \geq +1.8\, \text{A/mm}$ and $V_G \geq +6.0\, \text{V}$ for $>17.5$ hours is remarkable, in addition to the modest degradation in drain current that appears to saturate over stress time. The results reported herein are reproducible as evidenced by the similar responses of three devices, in addition to the fact that these parts are of standard commercial design from a baseline fabrication process. The results observed indicate that the GaN HEMTs tested are extremely robust to high forward gate bias and current. Devices based on the tested structure show the potential to withstand the rigors of forward gate bias and current during RF operation, and the high $I_G$ tolerance seen may allow extra latitude to circuit designers. Further investigations are required to understand the time-temperature-$V_G$ trade space and the full extent of degradation due to high forward bias and current under RF operation and over very long time periods (thousands of hours).

Disclosure

The views expressed in this paper are those of the authors and do not reflect the official policy or position of the United States Government.
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